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THE MAGAZINE FOR QUALITY IN ELECTRONICS




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Page 29

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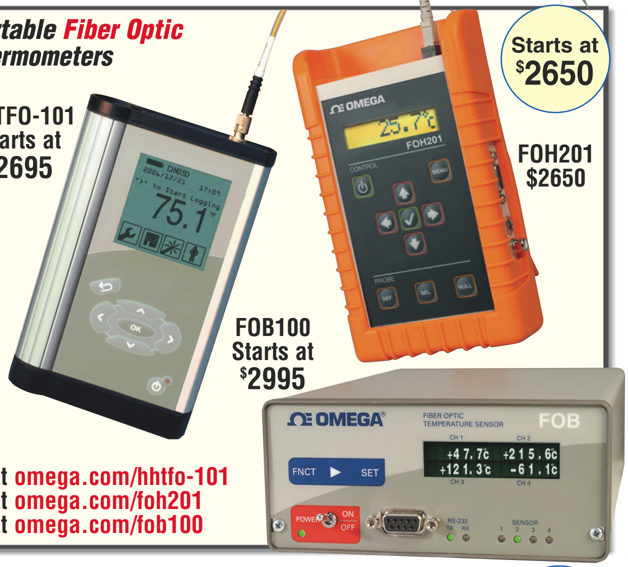


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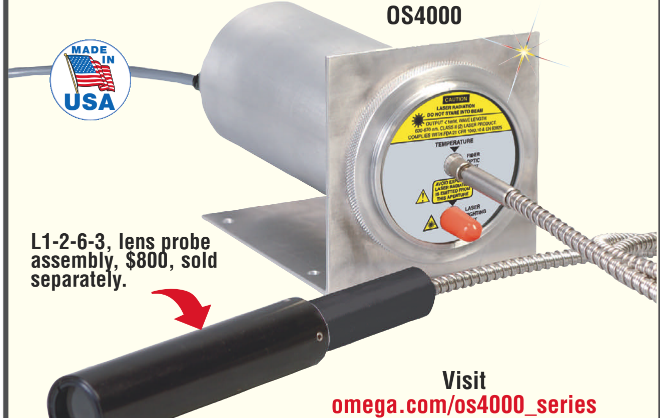

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VOL. 29 NO. 11

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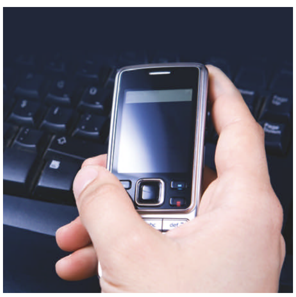

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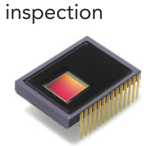

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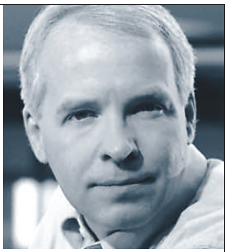

# EcoCAR sponsors help students

Last month, I commented on government efforts to support engineering education through STEM initiatives; this month, credit goes to private industry as well, which is supporting the DOE (Department of Energy) EcoCAR Challenge program, in which college students compete to redesign and rebuild a Saturn Vue to minimize fuel consumption and emissions.

Sponsors, including The MathWorks, National Instruments, Freescale Semiconductor, A123 Systems, and dSPACE, as well as GM, are helping students at 17 universities learn the latest techniques in electrical and mechanical design and simulation. The three-year program is now in its second year, with teams having conducted extensive design and simulation work during the first year while waiting for the arrival of the vehicles they plan to rebuild. At the end of year 2, the teams will have completed a "mule vehicle," borrowing GM's term for a prototype that's 60 to 65% of the way to being production-ready.

**Program builds the engineers who will build the vehicles of the future.**

Chad Conway, a sophomore double major in ME and EE, who serves as the electrical team leader for the Rose-Hulman EcoCAR team, says team members have been looking forward to year 2, when they begin taking wrenches to their vehicle, which arrived this fall. But Zac Chambers, associate professor of mechanical engineering and coadviser for the institute's EcoCAR program, says one thing participants can learn is patience: "A really big mistake that teams can make is that they immediately start tearing the vehicle apart. When they have an operational vehicle, it really behooves teams to use their CAN analysis tools to tap into the vehicle network to make sure they can communicate with all the different modules inside the vehicle and go out and collect some baseline data. They should get their testing procedures figured out while they have something that works before they try to figure out a testing procedure with something that may or may not work all that well."

During the first year, students conducted extensive model-based design (Ref. 1)—a technique heavily emphasized in the EcoCAR program, says Mike Wahlstrom, a control and simulation engineer at the Center for Transportation Research, Energy Systems Division, Argonne National Laboratory, which manages the EcoCAR program for the DOE. Says Wahlstrom, "This is a process that is really cutting edge in the auto industry right now. GM utilizes it, and that's why we thought it was really important to encourage it in EcoCAR."

And training in model-based design isn't only available to EcoCAR participants. Chambers says that Rose-Hulman, with help from The MathWorks, Freescale, and MotoTron, has established the first-in-the-nation collegiate-level model-based design laboratory and offers a beginning course in model-based design and an advanced course that covers hardware-in-the-loop testing.

Concludes Wahlstrom, "This is 100% about the students…we are not out here to change the world with any one vehicle that we are going to build in the competition. The great thing is that we are building the engineers that will build those vehicles in the future." T&MW

## REFERENCE

1. Nelson, Rick, "Model-based design and early verification aid designers," *EDN*, December 15, 2009. www.edn.com/article/CA6711858.html.

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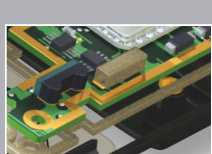


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## EDITORIAL STAFF

**Editor in Chief:** Rick Nelson
rnelson@tmworld.com
*ATE & EDA, Inspection, Failure Analysis, Wireless Test, Software, Environmental Test*

**Managing Editor:** Deborah M. Sargent
dsargent@tmworld.com

**Senior Technical Editor:** Martin Rowe
mrowe@tmworld.com
*Instruments, Telecom Test, Fiber-Optics, EMC Test, Data-Analysis Software*

**Assistant Managing Editor:** Naomi Eigner Price
neprice@tmworld.com

**Contributing Technical Editors:**

Bradley J. Thompson, brad@tmworld.com

Steve Scheiber, sscheiber@aol.com

Richard A. Quinnell, richquinnell@att.net

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**Editorial Intern:** Jennifer Kempe

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## HOW TO CONTACT T&MW

**EDITORIAL:**
225 Wyman St.
Waltham, MA 02451

Phone: 781-734-8423
Fax: 781-734-8070
E-mail: tmw@reedbusiness.com
Web: www.tmworld.com

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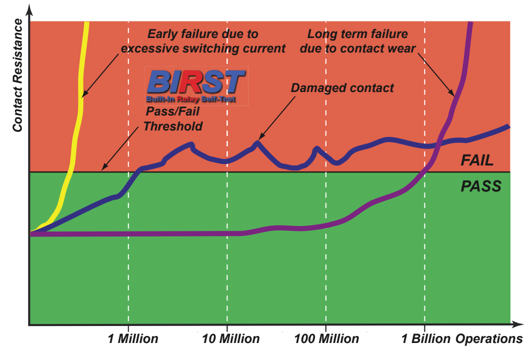


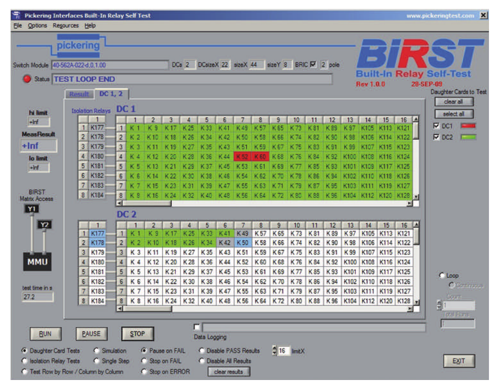


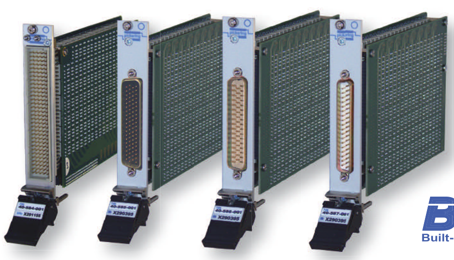

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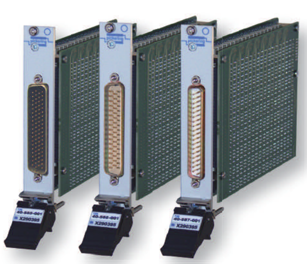

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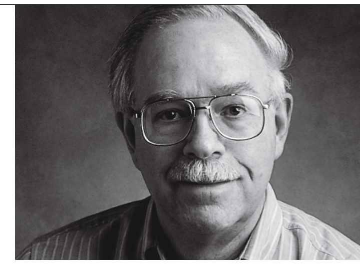
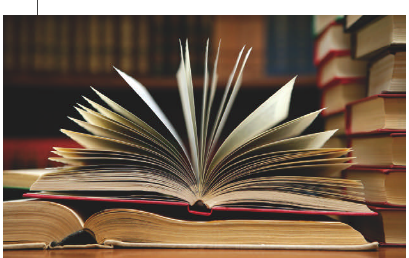


# Winter reading: windmills and prostheses

Winter has arrived here in the northern hemisphere, and with it the indoor entertainment season. Serendipitous connections to the world of electronic test and measurement are welcome but optional, and you need no excuse to kick back and read a book.

One young African man did just that. Faced with a life that promised no further schooling, repeated bouts of near starvation, brushes with cholera, and a "career" as a subsistence farmer, William Kamkwamba visited his local library, a branch sponsored by the Malawi Teacher Training Activity and stocked with books donated by USAID (US Agency for International Development).



Intrigued by a textbook illustration of a windmill, Kamkwamba envisioned what electricity could mean for his family—nighttime illumination, power for a sewing machine, and a well pump that could free his mother and sisters from walking miles to fetch water for the family.

If you read Kamkwamba's book, *The Boy Who Harnessed the Wind,* as his autobiography, you'll meet an extraordinary human being. Read the book as a technical account, and you'll appreciate the importance of having a junkyard and a library nearby. As for his test equipment, can you do your job equipped only with sparks and salvaged incandescent lamps? To quote Anne Herbert, "Libraries will get you through times of no money better than money will get you through times of no libraries" (Ref. 1).

At the other extreme, a small fraction of the US Department of Defense budget (approximately 0.4%) funds DARPA (Defense Advanced Projects Research Agency). Presumably, DARPA's scientists and engineers enjoy access to proportionately large junkyards and libraries. Funding for research, development, test, and evaluation activities alone exceeds $200 million. DARPA also tackles projects far beyond the scope of any individual's efforts.

In his book *The Department of Mad Scientists*, author Michael Belfiore explores DARPA-sponsored development of prosthetic limbs for wounded military personnel, the Internet, robotic surgical suites, autonomous motor vehicles, and jet-engine grade fuels derived from soybeans. All of these activities have obvious military uses, but odds are excellent that, like the Internet, they'll eventually serve the civilian world. T&MW

## REFERENCE

1. Anne Herbert, as quoted in *The Next Whole Earth Catalog: Access to Tools*, Stewart Brand (ed.), Random House, New York, 1980. Herbert derived this quotation from cartoonist Gilbert Shelton's aphorism regarding recreational drugs and money.

To read past "Test Voices" columns, go to www.tmworld.com/testvoices.

## SUGGESTED BOOKS

*The Boy Who Harnessed the Wind: Creating Currents of Electricity and Hope*, by William Kamkwamba and Bryan Mealer. HarperCollins, New York (www.harpercollins.com), 2009. 273 pages.

*The Department of Mad Scientists: How DARPA Is Remaking Our World, from the Internet to Artificial Limbs*, by Michael Belfiore. HarperCollins, New York (www.harpercollins.com), 2009. 295 pages.

For more information about DARPA and its budget, go here:
www.darpa.mil/about.html
www.darpa.mil/budget.html

## MISCELLANEA

Is your camera smart enough to augment a T&M setup? CHDK (Canon Hack Development Kit), a free package of firmware extensions for Canon digital cameras incorporating Digic II through Digic IV operating systems, enables time-lapse and strobe photography and remote control via USB.
chdk.wikia.com/wiki/CHDK

Beyond its other services, Google conducts research in various areas, including hardware reliability, as covered in this paper: "Failure Trends in a Large Disk Drive Population," by Eduardo Pinheiro, Wolf-Dietrich Weber, and Luiz André Barroso. Proceedings of the 5th USENIX Conference on File and Storage Technologies (FAST 2007), San Jose, CA, February 2007. You can read the paper here:
labs.google.com/papers/disk_failures.html

NKC Electronics offers a fully assembled digital storage oscilloscope for $49, or in kit form for $35.95. While its 5-Msamples/s digitizing rate, 8-bit resolution, and 256-byte sample memory won't cause heartburn in Beaverton or Santa Clara, this little Chinese-made instrument might enhance your test lash-up:
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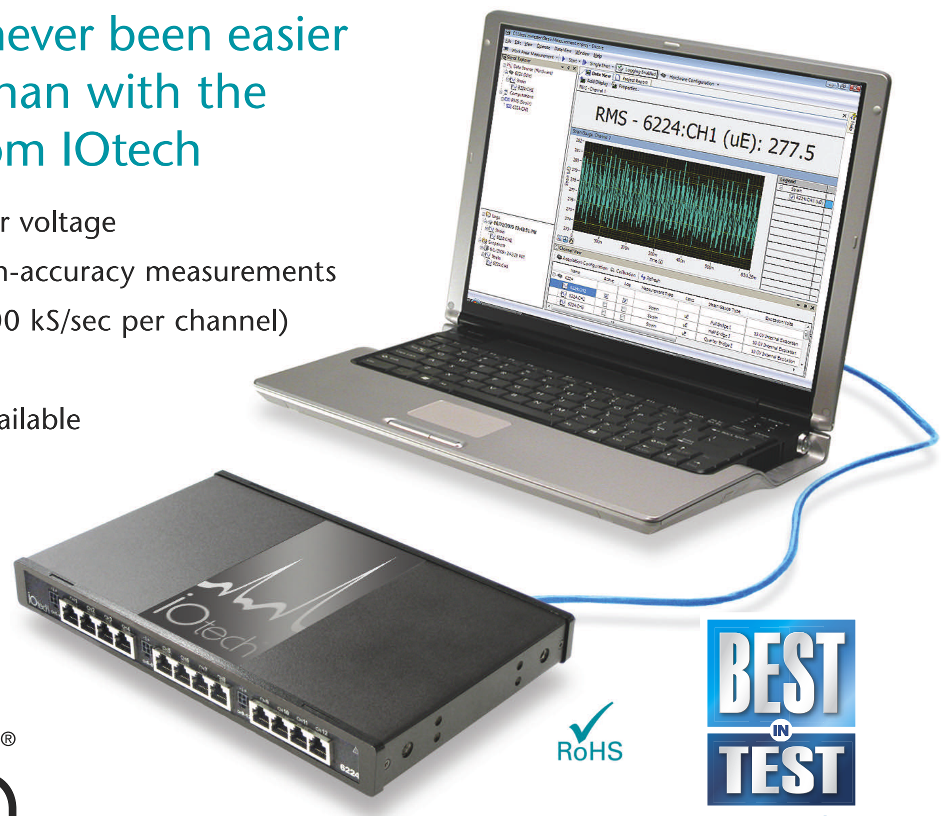


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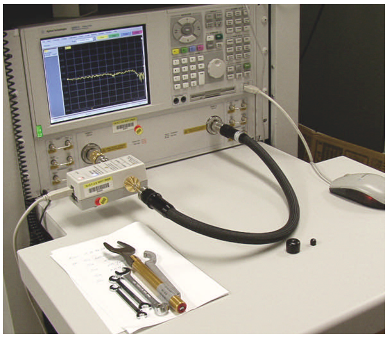
## NIST automates verification of VNA calibrations

Engineers at NIST (National Institute of Standards and Technology) report they have devised a new method for verifying the calibration of VNAs (vector network analyzers). The engineers have developed an electronic verification standard and accompanying software that automate the verification process and provide results in minutes rather than hours or days.



The new procedure replaces the method in which engineers verified a VNA's calibration by plugging a series of mechanical artifacts with different, known performance characteristics into the instrument, running tests on each artifact, and recording the results. Instead, engineers need only one computer-controlled electronic verification artifact that can switch to numerous predefined impedance and transmission states. NIST's VeridiCal software automates the process and enables users to log results to NIST servers over the Internet.

"Every time a vector network analyzer, a common electrical measurement instrument, took a measurement, it would measure eight different parameters at once and you were never sure if it was measuring them all correctly," said NIST electronics engineer Dylan Williams in a prepared statement. "It has been a nagging problem for some time with no real way to check it. Now, you can verify the performance of your analyzer and cover the whole space of what the instrument can measure." www.nist.gov.

## Agilent acquires Keithley's RF line

Keithley Instruments has sold the bulk of its wireless test equipment product line to Agilent Technologies. The deal, which involved the transfer of Keithley's RF design center in Santa Rosa, CA, reportedly garnered Keithley $9 million. The facility employed about two dozen people, who were expected to be offered jobs with Agilent. Agilent will provide global sales, service, and support for the existing RF product line.

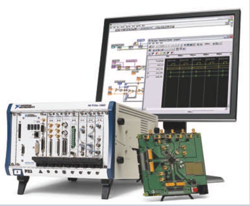
"Because we have placed a high emphasis on profitability in fiscal 2010 and beyond, we concluded that we could no longer continue to support our significant investment in RF measurement products, and should instead focus on growing our core business," stated CEO Joseph Keithley. "The impact of the economic downturn changed the expected timing of the returns we were anticipating from our RF product line, extending them beyond a time frame that we were willing to continue to support. We are pleased that Agilent will be assuming this product line. Both Keithley and Agilent will work to provide high-quality service and support through the transition for our customers using these products."

Keithley added, "We remain committed to supporting our customers in the semiconductor, wireless, precision electronics, and research and education industry segments, serving applications in research, development, and production. The divestiture of our RF product line enables us to increase our focus on our core technologies, and we intend to expand our efforts to

## NI targets semiconductor test

Editors' CHOICE

National Instruments has introduced 10 products that expand the capabilities of PXI for mixed-signal semiconductor test. The NI PXI Semiconductor Suite includes four HSDIO (high-speed digital I/O) instruments, two digital switches, two RF instruments, an SMU (source-measure unit), and digital-vector file-importing software. It incorporates 200-MHz single-ended digital I/O, 10-pA current resolution, multiband RF measurements, and DC/digital switching. The tools target semiconductor characterization, addressing ADCs, DACs, power-management ICs, wireless ICs, and MEMS devices.



The NI PXIe-654x HSDIO instruments offer single-ended clock rates up to 200 MHz and data rates to 400 Mbps. The NI PXI-4132 SMU delivers current sensitivity down to 10 pA. The NI PXI-2515 and NI PXIe-2515 digital switches help users multiplex DC instrumentation onto HSDIO lines. The NI PXIe-5663E and NI PXIe-5673E 6.6-GHz vector signal analyzer and vector signal generator offer increased measurement speed through deterministic changes in RF configurations. The new suite also permits the importing of WGL and STIL digital-vector formats to streamline design-to-test integration when using NI PXI high-speed digital products.

Base prices: $2499 for a high-speed digital signal insertion switch to $23,999 for a 6.6-GHz RF vector signal generator. *National Instruments, www.ni.com.*

## BERT reaches 25-Gbps data streams

Editors' CHOICE

Synthesys Research has expanded the speed and bandwidth of its BERTScope to let you make physical-layer measurements on 25-Gbps lanes for IEEE 802.3ba, 100-Gbps Ethernet. (802.3ba specifies four 25.781-Gbps lanes for 100-Gbps operation.) The BERTScope 25000A ($250,000) and BERTScope Si 25000C ($300,000) let you measure BER (bit-error rate) and perform jitter analysis on 100GBASE-LR4/ER4 transceiver modules, boards, and systems.

The Si model adds stress-receiver testing to the base model. That lets you stress receivers with sinusoidal jitter, random jitter, bounded uncorrelated jitter, and phase modulation.

The BERTScope is capable of testing data streams up to 26.781 Gbps, providing a measurement safety margin. To reach that speed, Synthesys engineers had to design a custom SiGe chip. With that technology, Synthesys has also increased the speed of its BERTScope CR clock-recovery unit to 26 Gbps.

The BERTScope 25000A and Si 25000C include a linear equalization feature that removes distortion from an incoming data stream. With that feature, the instrument's clock-recovery unit can restore the clock embedded in the data.

*Synthesys Research, www.bertscope.com.*


leverage these strengths in support of new growth opportunities such as energy efficiency related devices and materials." www.keithley.com; www.agilent.com.

## Chartered enhances yield management

Chartered Semiconductor Manufacturing reports that it has begun the next phase of expansion, equipment move-in, and installation for its most advanced manufacturing facility, Fab 7—a 300-mm wafer fab. The equipment will support the planned ramp of capacity for the company's leading-edge process offerings of 65-nm and 45/40-nm technology.

Chartered Semiconductor plans to approach a production level of approximately 50,000 wafers per month by the time the equipment is completely installed and operational. The current expansion phase will add an additional 50,000 $ft^2$ of clean-room space to Fab 7, an increase of 23%.

Fab 7 benefits from comprehensive yield management and defect detection systems. The fab uses intelligent computer-integrated manufacturing systems, advanced process control, fault detection, and classification and recipe management systems. www.chartered-semi.com.

## CALENDAR

**OFCNFOEC,** March 21–25, San Diego, CA. *Optical Society of America. www.ofcnfoec.org.*

**Measurement Science Conference,** March 22–26, Pasadena, CA. *Measurement Science Conference. www.msc-conf.com.*

**APEX,** April 6–9, Las Vegas, NV. *IPC. www.goipcshows.org.*

**SAE World Congress,** April 13–15, Detroit, MI. *SAE International. www.sae.org.*

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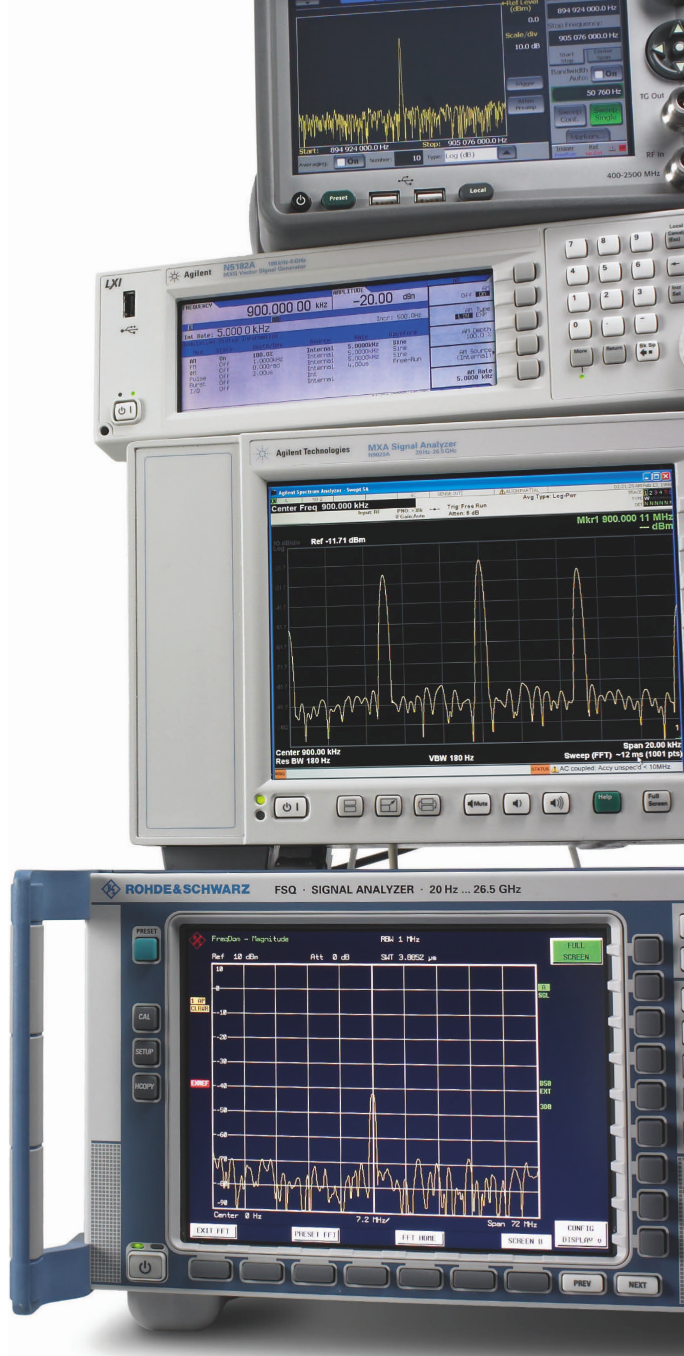


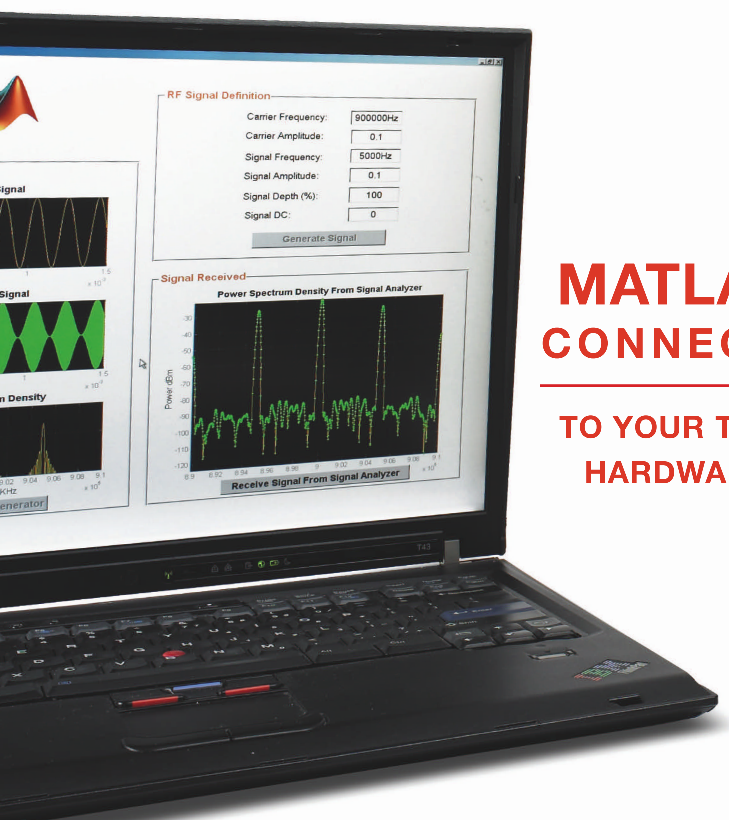


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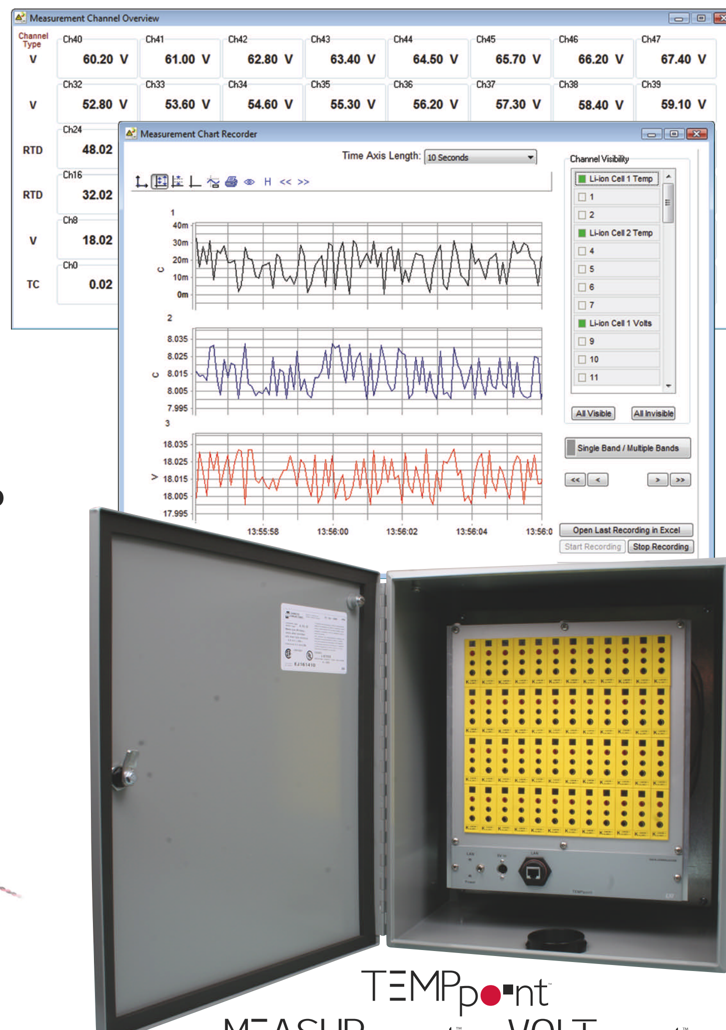


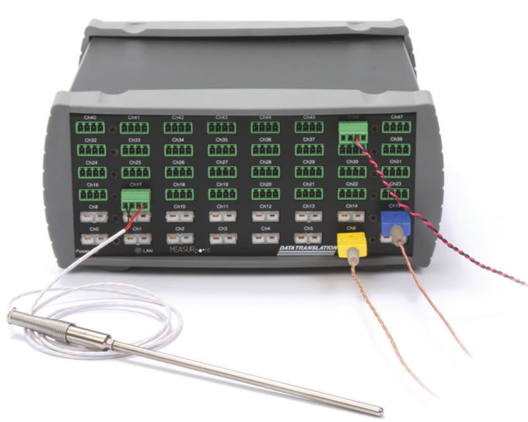

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# Vendors tout cameras, interfaces, and processing

> > > Vision 2009, November 3–5, Stuttgart, Germany, www.messe-stuttgart.de/vision.

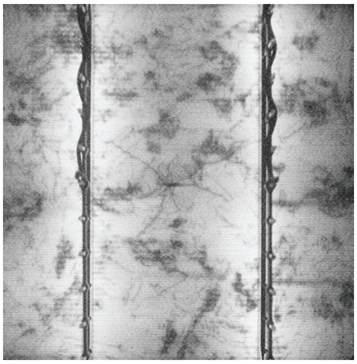
**Baumer** presented its new HQ Color technology, based on the real-time Baumer CIELab engine. Baumer also presented its new GigE trigger device and introduced the SX family of cameras, which incorporate **Kodak**'s progressive-scan interline CCD sensors. **Basler Vision Technologies** introduced its low-cost (299 euros) Ace GigE camera, a 29x29-mm unit.

**Matrox Imaging** announced two PICMG 1.3 boards for its Matrox Supersight e2 HPC (high-performance computing) platform. Matrox also said that the Matrox Radient eCL Camera Link frame grabber now supports the Altera Stratix IV FPGAs.

**Dalsa** highlighted its Spyder3 linescan cameras; its Falcon VGA300 HG, Falcon 1M120 HG, and Falcon 1.4M100 HG cameras; its BOA smart camera; and two new Genie GigE Vision-compliant cameras. Dalsa also demonstrated its Sapera Essential measurement tool, the Xcelera CL PX8 frame grabber, and the XRI-1600 PC-based digital image processor. In addition, Dalsa presented its HSLink high-speed interface.

Proposing another high-speed link called CoaXpress were **Active Silicon, Adimec,** and **Components Express;** the **Japanese Industrial Imaging Association** (JIIA) will address CoaXpress standardization issues. Also, representatives of the JIIA, the **Automated Imaging Association**, and the **European Machine Vision Association** signed an agreement to cooperate on global machine-vision standards.

**Vision Components** presented its VCSBC4012 nano intelligent board camera and its VC4012 nano enclosed camera. Vision Components also said it is enabling cost-efficient production and quality control in the solar industry by combining its VC Solar Solution software library with smart cameras such as the new VC4067/NIR near-infrared model. The company also hosted application providers at its booth: **Sedeco Vision Components** presented its interfacing tools, which enable the operation of **MVTec**'s HALCON on VC Smart Cameras; **FiberVision** exhibited its VC-Smart-Camera-based Caminax and its Nanosmart-PoE (Power over Ethernet) intelligent camera with a 5-Mpixel resolution; and **IBN** presented its PICTOMAT camera systems used in a 3-D volume calculation application and a camera-guided pick-and-place robot application. T&MW



**Vision Components' VC4067/NIR captured this near-infrared image of a polycrystalline wafer with microcracks in the center. Featuring an integrated 400-MHz processor from Texas Instruments, the camera has a computing power of 3200 MIPS.**

Courtesy of Vision Components.

# New failure mechanisms, analog, and adaptive test

> > > International Test Conference, November 2–5, Austin, TX, www.itctestweek.org.

Forward-looking issues grabbed center stage from the start of the International Test Conference this year, beginning with the keynote addresses. Antun Domic, senior VP and GM at Synopsys, described the parallel evolution of test challenges and test tools. Challenges, he said, had progressed from finding stuck-at faults to fighting test complexity to wrestling power and timing in test circuits to—tomorrow—facing whole new kinds of faults. In response, Domic suggested, tools have evolved from being point solutions, to offering test-aware synthesis, to integrating test into design flows to fight power and timing issues. Tomorrow, he said, these full test flows will require timing, physical design, and process information as well.

Looking even farther ahead, Intel fellow Shekhar Borkar described the chip of the future: a massive mesh of small soft IP blocks, each with fine-grained voltage scaling, operating near the transistors' threshold voltage. The resulting soft error rates, added to extreme process variations and aging effects, would render factory testing meaningless, Borkar said. Instead, designs would have to self-test on the fly, and then self-calibrate and reconfigure. This view upends the traditional role of test in the design flow entirely.

Later, in an analog session, panelists queried whether analysis could collapse a full parametric sweep into a set of point measurements, and whether such concepts as built-in self-test and structural test—fundamental in the digital world—could apply to analog circuits. The answers depended on accurate analog fault models and much better R&D funding.

In an adaptive test panel, panelists first tried to define adaptive test, homing in on the ability to eliminate tests from the program based on the emerging statistics from previous tests. One debate that sprung up was whether or not adaptive test—based as it is on histories of individual chip test results—required each die to have a unique serial number. T&MW

# Lab and characterization tools debut at Productronica

>>> Productronica, November 10–13, Munich, Germany, www.productronica.de.

**National Instruments** debuted 10 new PXI products with associated software that target semiconductor characterization.

**Aeroflex** highlighted its 7000 Series VAG (vector analyzer generator), a single, integrated RF parametric test system for RF test of wireless components and subsystems.

**JTAG Technologies** debuted its JTAG Live family: Buzz replaces the audible continuity test of traditional DMMs or allows oscilloscope-like probing; Clip acts as a logic analyzer, applying vector-based cluster tests; and Script enables users to employ the **Python** language to take control of a design through onboard boundary-scan compliant devices. To connect to a board-under-test, family members are compatible with the JTAG programming cables from **Altera** and **Xilinx**.

**Rohde & Schwarz** debuted a new signaling capability for its CMU500 production tester. Rohde & Schwarz also presented a system for generating phase-coherent multichannel signals for testing radar receivers.

**Spectrum** introduced the M3i.21xx series digitizers, which operate to 1 Gsample/s with one or two synchronous channels. **Viscom** debuted its S3088-III AOI system, which is optimized for solder-joint inspection on boards measuring 20x20 in. **Test Research** introduced its TR7007 solder-paste inspection system, which incorporates the company's 64-bit 3-D technology. **Vötsch Industrietechnik** highlighted a temperature test chamber with EMC shielding.

For radar test applications, Rohde & Schwarz presented a system combining R&S signal generators in a flexible PXI-compliant test system.
Courtesy of Rohde & Schwarz.

Aeroflex, **Agilent Technologies**, and **Test Evolution** proposed a new modular test standard, AXIe (AdvancedTCA Extensions for Instrumentation and Test), an open standard based on AdvancedTCA (ATCA). AXIe, proponents say, leverages existing standards from ATCA, PXI, LXI, and IVI organizations (see p. 24). T&MW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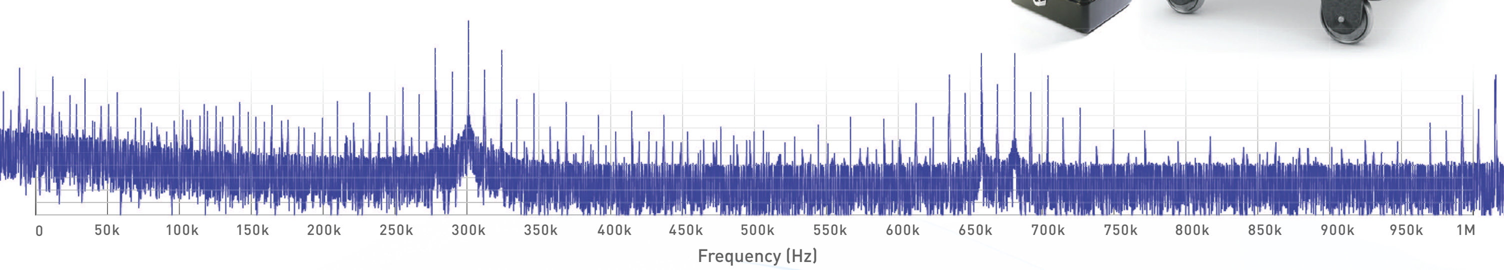


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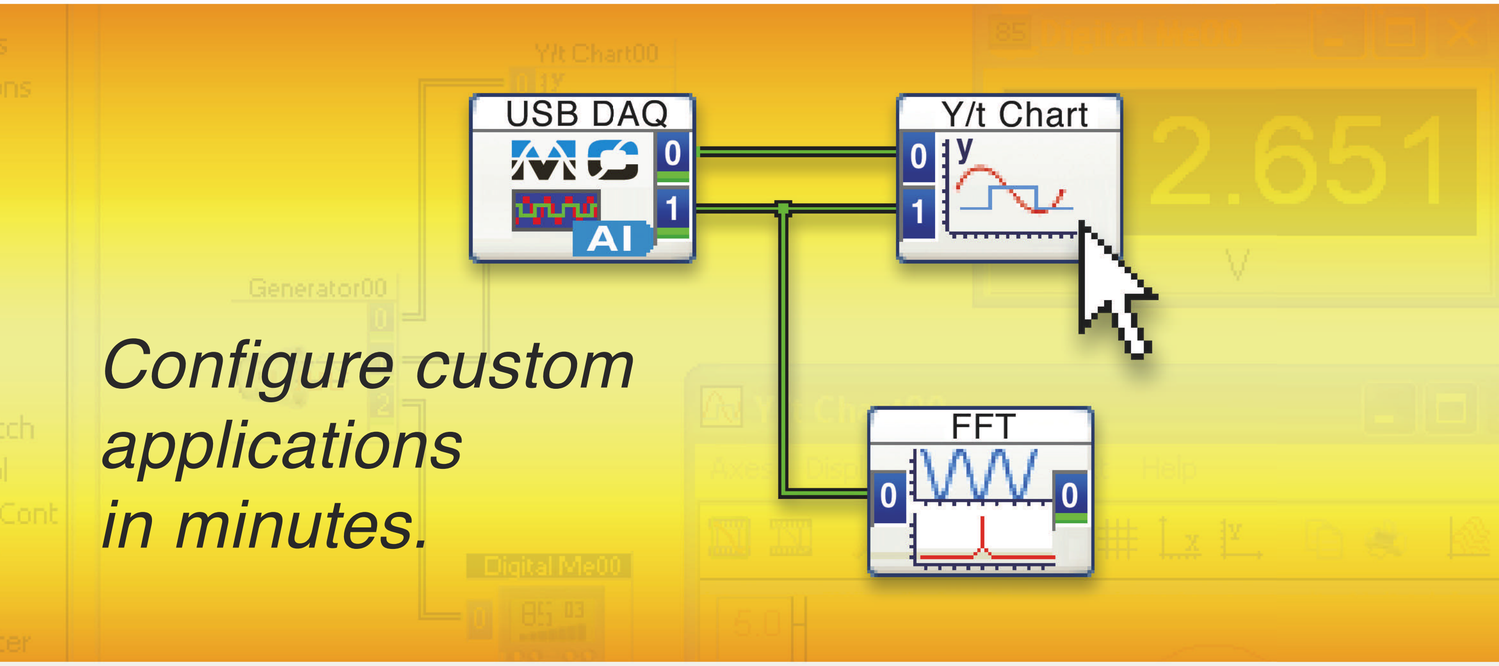


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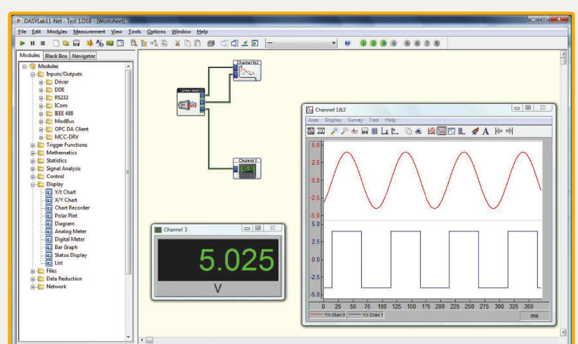


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MARTIN ROWE
SENIOR TECHNICAL EDITOR
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# Smartphones tax mobile networks

First there were voice-over-wireless networks. Then came text, photos, and Web browsing, and now just about anything goes. Smartphones such as the iPhone let you download books, music, and videos and listen to steaming audio almost anywhere.

The bandwidth demands from these multimedia applications are staggering compared to those of voice and text: 10 Mbps versus 348 kbps, according to Sylvain Cornay, market development manager at EXFO. Thus, you can conclude that smartphones, the iPhone in particular, use a disproportionate share of mobile bandwidth.

AT&T, which bears the brunt of the iPhone bandwidth demand, has announced network upgrades and plans to implement LTE into its networks in 2010 (Ref. 1). LTE uses IP (Internet Protocol) over the entire network, from the wireless interface to the network core. LTE will let even more applications run on handsets.

"Applications put pressure on the mobile backhaul because current technology can't scale to meet bandwidth needs," said Vikas Arora, CTO of EXFO. "The increased bandwidth," added Paul Gowans, field marketing manager at Agilent Technologies, "doesn't increase revenue, which results in lower revenue per bit."

**The iPhone and other smartphones have produced a significant increase in demand for wireless bandwidth.**
Courtesy of Apple.

Joe Mader, director of marketing for wireless and core network testing at Spirent Communications, noted that downloading songs and video and listening to streaming audio forces the handset to keep its "bearer channels," which carry the data between the handset and the network core, active for long periods. That also puts strains on a network, because it can't release the bandwidth to other users.

Nigel Wright, Spirent's mobile device test group VP, explained that carriers look for handsets that make the most of network bandwidth. Thus, they test the bandwidth efficiency of a variety of handsets and sell the ones that do the best job. Handset testing involves emulating a wireless network, testing for call setup and breakdown, and testing for dropped calls.

Because handsets incorporate multiple functions, carriers must decide which functions to test. For example, they might test for voice quality or dropped calls when a handset receives e-mails.

Smartphone applications have forced carriers to look at networks differently. "Carriers can no longer look at protocols and low-level interoperability," said Adam Fowler, VP of product management for wireless at Ixia. "They must test QoS [quality of service] and QoE [quality of experience]." Such testing includes verifying that networks meet user contracts for bandwidth. Carriers must also test for audio and video quality, the same as they do for wireline voice and video over IP networks.

The greater bandwidth demands also take a toll on cell towers, which must seamlessly pass a user as the user moves. Bandwidth demands in cities also increase as people commute to work in the morning and lessen when they leave at night. But the towers along commuter routes take the burden during commuting hours. Cell towers also receive heavy loads during large conventions and sporting events. EXFO's Arora noted that carriers need to perform end-to-end testing to ensure end-user QoE under heavy load conditions. T&MW

## REFERENCE

1. "AT&T to Deliver 3G Mobile Broadband Speed Boost," press release, May 27, 2009. www.att.com/gen/press-room?pid=4800&cdvn=news&newsarticleid=26835.

To read past "Tech Trends" columns, go to www.tmworld.com/techtrends.

### USB-controlled filter offers 90-dB attenuation

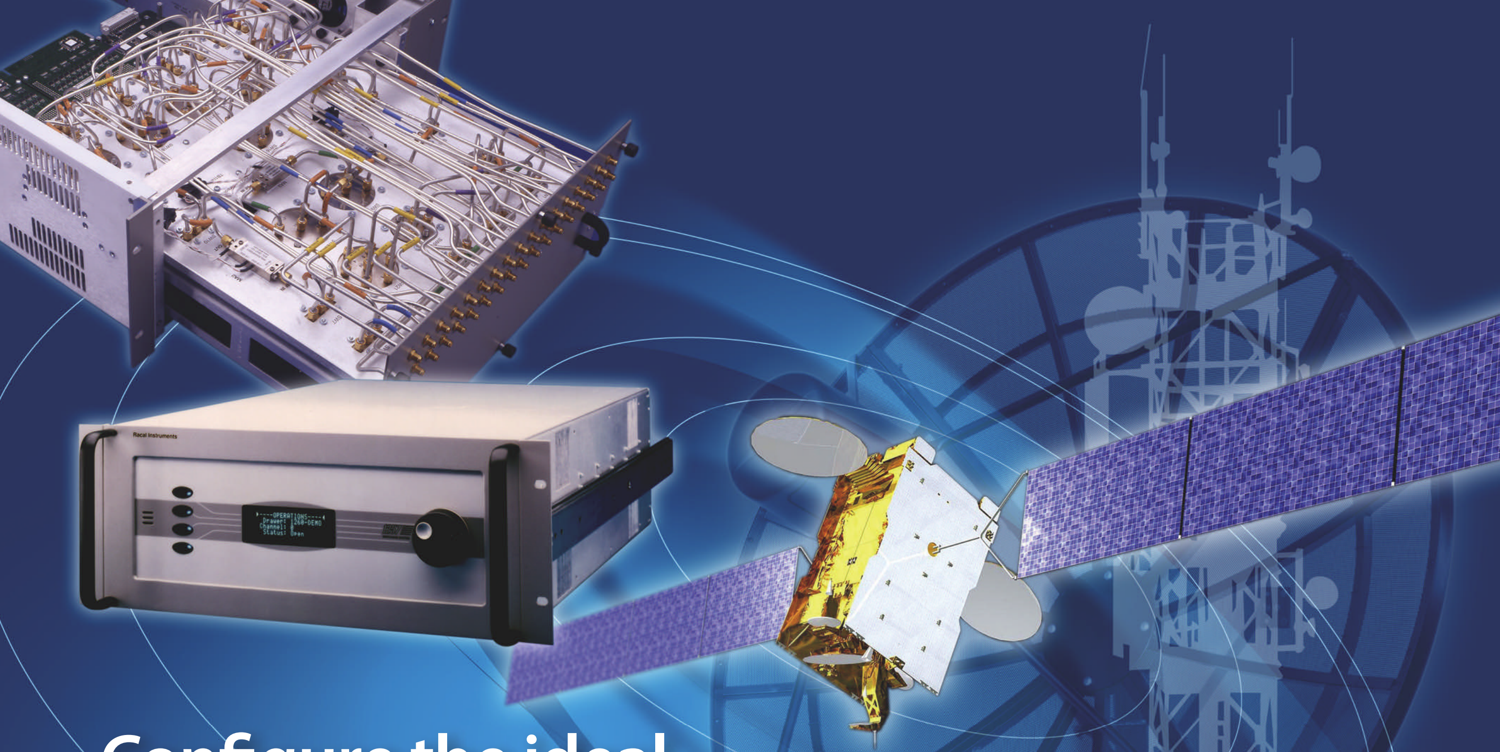
The USBPGF-S1 instrumentation amplifier and eight-pole low-pass filter is programmable from 0.1 Hz to 200 kHz with 90-dB attenuation. Filters include Bessel, Butterworth, Cauer/elliptic, and linear phase. The USBPGF-S1 stores its configuration in nonvolatile memory. www.alligatortech.com.

### Logic analyzer adapter targets communications devices

The LA-BGA-LPDDR-SDRAM-01 adapter lets you analyze memory devices in PDAs, cellphones, digital cameras, and MP3 players with a logic analyzer or oscilloscope. www.ironwoodelectronics.com.

### DAQ system gains a synchro/resolver interface board

UEI has added a two-channel synchro/resolver board to its PowerDNA "cube" Ethernet data-acquisition system. Each channel has an independent 16-bit ADC and has ±2.6 arc-min accuracy. www.ueidaq.com.

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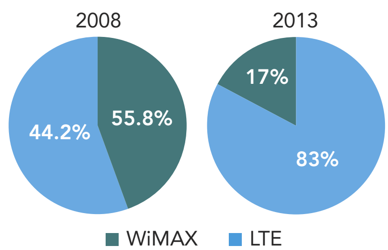
## WiMAX and LTE—4G-ing ahead

With Qualcomm discontinuing development of its UMB (Ultra Mobile Broadband) technology in November 2008, the competition for the coveted 4G wireless title is down to a two-horse race: WiMAX and LTE. These technologies, capable of delivering fixed and mobile high-speed data services, have the communication industry wondering which is the best solution for mobile broadband.

Despite the media hype, intense debates, and expected comparison to the GSM vs. CDMA rivalry, WiMAX and LTE have more similarities than differences. They both claim to outperform 3G with data speeds of up to 100 Mbps and have the potential to replace wired broadband connections.

Consumer demand for true mobile broadband wireless communications has accelerated the evolution to 4G technologies. Although WiMAX evolved from Fixed WiMAX and LTE evolved from GSM, SPRS/EDGE, UMTS, and HSPA technologies, they both apply OFDMA (orthogonal frequency-division multiple access) and MIMO (multiple input, multiple output) technology to improve system capacity and reduce signal latency. Both technologies are also IP-based instead of mobile-phone-network based.

Where the two technologies do differ is in their development life cycle. WiMAX is available today, with the WiMAX Forum claiming there are over 455 WiMAX networks deployed in more than 135 countries. LTE, on the other hand, is still in its testing phase, with Verizon Wireless announcing trial networks at the end of 2009 with a first commercial launch planned for 2010; mass commercial deployments are not expected until 2012.




**Although holding a smaller market share than WiMAX in 2008, LTE is expected to grow significantly in the next few years.**

Just as GSM's dominance of the global cellular marketplace is attributed to its early deployment in comparison with CDMA, WiMAX loyalists have reiterated that its head start over LTE has already decided the fate of this 4G race. LTE forerunners, however, will be quick to point out that LTE is the natural evolution of GSM/EDGE and UMTS/HSPA networks, which account for 80% of mobile subscribers globally, a crucial advantage that negates WiMAX's first-mover advantage.

WiMAX and LTE will play vital roles in their own way and are more likely to coexist than compete. From a test and measurement perspective, the advantage is clearly with LTE, just by virtue of the backing it enjoys from a number of leading carriers across the globe. LTE is also in its development stage, creating testing opportunities that cover the full LTE development life cycle, from early R&D device and base-station testing to monitoring and installation and maintenance applications. Although the R&D phase for WiMAX is over, test equipment vendors still see growth opportunities. The demand for mobile WiMAX devices is growing, and more networks are deployed across the globe, helping countries bridge the digital divide, particularly in emerging nations. T&MW

To read past "Market Trends" columns, go to www.tmworld.com/markettrends.

### Capital equipment spending to grow 45% in 2010

Worldwide spending on semiconductor equipment may be expected to end 2009 down more than 42%, but it is expected to bounce back with more than 45% growth in 2010, according to the latest data from Gartner (www.gartner.com).

Specifically, the research company has reported that the year is expected to show a 42.6% decline as compared to 2008. But, said Gartner, the market is now in the midst of a very strong growth spurt, and semiconductor equipment spending is expected to increase 45.3% in 2010.

"Foundry spending and select spending by a few memory companies drove the growth in the semiconductor equipment segment in the second half of 2009," said Dean Freeman, research VP at Gartner. "2010 growth will be driven by technology upgrades for the first half of the year. The quarterly growth may see a slight lull in the third quarter of 2010 before capacity additions, starting in late 2010, ramp up the equipment industry into 2011."

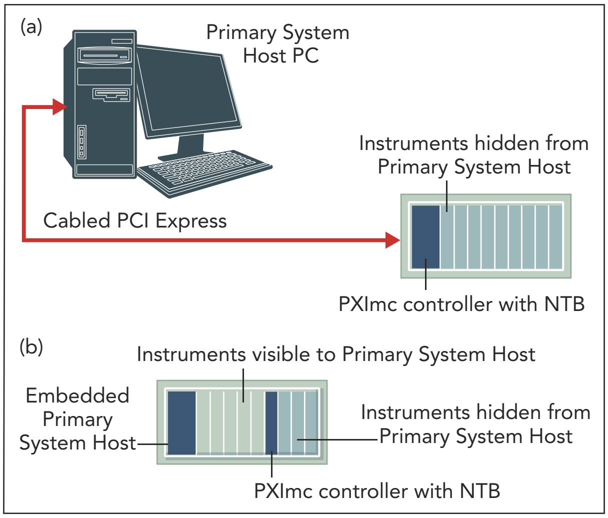
While all segments of the semiconductor equipment market experienced significant declines in 2009, all segments of the market will experience strong double-digit growth in 2010, Gartner said.

Indeed, worldwide wafer fab equipment spending is expected to decrease 48.1% in 2009, but to increase 56.6% in 2010. Worldwide packaging and assembly equipment spending is forecast to decrease 40.5% in 2009, then increase 52.8% in 2010. And worldwide automated test equipment is on pace to decline 44.9% in 2009, but is expected to be followed by growth of 59.7% in 2010.

*Suzanne Deffree, Managing Editor, News,* EDN

PC-BASED INSTRUMENTS

# PXI expands to multiple processors




**In (a), a cabled PCIe link connects a PC to a PXImc host controller, which hides all instruments from the PC. In (b), the PXImc controller hides some of the instruments from the embedded PXI controller.**

The PXI Systems Alliance has announced the PXImc (PXI MultiComputing) specification in two parts: hardware and software. Systems that comply with the new specification can have more than one processor module, thus increasing computing power.

Think of PXImc as a local network for PXI/PXIe (PXI Express). A PXImc system's primary controller, called a Primary System Host, can communicate with a PXImc processor device over a PCI backplane, a PCIe (PCI Express) backplane, or a cabled PCIe port through an NTB (nontransparent bridge). With an NTB, the host controller can see only the PXImc device and instruments connected directly to the host—it can't see instrument cards across the bridge. Each PXImc device and the instruments behind it appear as a single PXI node to the Primary System Host. A PXImc device contains a processor, memory, a PCI/PCIe root complex, and an NTB.

The Primary System Host can be a stand-alone PC or a PXI/PXIe embedded controller. If the host is a stand-alone PC, it connects to a PXI/PXIe chassis through a cabled PXIe port. If the host is an embedded PXI/PXIe controller, it connects to a PXImc controller over the chassis backplane.

The **figure** shows two possible configurations. A PC connects to a PXI chassis where the chassis controller is a PXImc controller. In this configuration, the host can't see any of the instruments in the chassis. In the chassis with the embedded controller, the host can see some instruments and the PXImc controller, but it can't see the instruments beyond the PXImc controller.

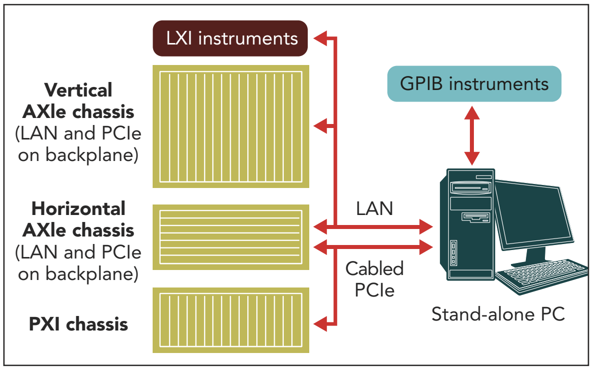
The PXImc specifications also let you expand your system beyond a single chassis. If you need a system with a PC as a primary host and need more than one instrument chassis or other PXImc-compliant device, you can connect the host to an external cabled PCIe switch to add ports.

You can download the PXImc hardware and software specifications at www.pxisa.org/Specifications.html.

*Martin Rowe, Senior Technical Editor*

PC-BASED INSTRUMENTS

# Instrument bus standard announced




**The AXIe standard uses backplane and cabled PCIe or LAN cards to connect instruments.**

Aeroflex, Agilent Technologies, and Test Evolution have formed an alliance to develop and promote AXIe (AdvancedTCA Extensions for Instrumentation and Test), a new instrumentation bus standard designed for both general-purpose and semiconductor test. The new standard combines three existing computer buses—ATCA (Advanced Telecom Computing Architecture), PCIe (Peripheral Component Interconnect Express), and LXI (LAN eXtensions for Instrumentation)—into a single platform.

The **figure** shows how instruments connect under the AXIe standard. An AXIe instrumentation chassis can hold 1 to 14 cards and uses Ethernet, PCIe, or both on its backplane for board communications. The AXIe 1.0 standard (Ref. 1) calls for both buses, but a chassis designer might choose only one. Instrument makers can design cards for either bus.

The slots in an AXIe chassis are large enough to hold ATCA cards, used in the telecom industry, which are larger than two 1U-sized PCIe or PXI cards. Adapter cards will hold one or two PCIe/PXI cards, adapting new or existing instrument cards to either backplane bus.

An AXIe chassis will also have cabled LAN and PCIe ports. The cabled PCIe bus in an AXIe chassis connects a host controller to a PCIe or PXI chassis. The LAN ports can connect the chassis to a host controller PC, which can also support external LAN-based LXI instruments.

Through an interface card, the host can also communicate with GPIB instruments, so you can protect your investment in those instruments if you decide to use AXIe. The AXIe standard will let you use your existing instrument drivers, be they PXI, LXI, or IVI (interchangeable virtual instrument). The instrument bus should be transparent to your application software.

*Martin Rowe, Senior Technical Editor*

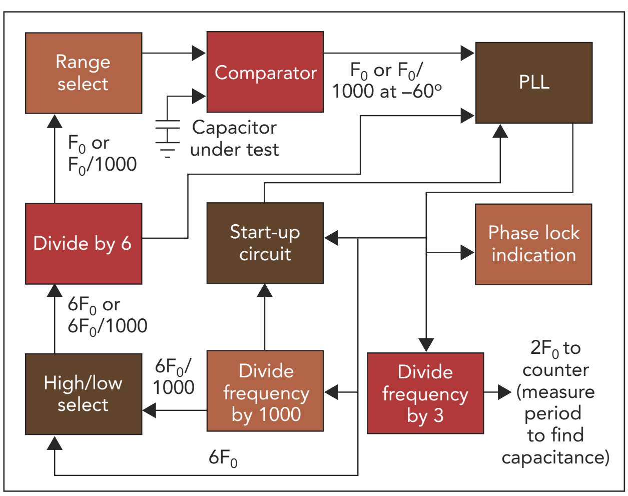
REFERENCE


1. AXIe Consortium. www.axiestandard.org.


INSTRUMENTATION

# Build your own capacitance meter

If you need to measure capacitance but don't have the necessary meter, you may be able to build a circuit that can handle the task. For example, if you have a data-acquisition board or module that measures frequency or signal period, you can build a circuit that converts capacitance to frequency and then measure the period with a counter.




**This block diagram illustrates a capacitance meter that can measure from 10 pF to 10 μF with ±1-pF accuracy.**

**Figure 1** shows the block diagram that engineer Jim McLucas developed for a capacitance meter that can measure from 10 pF to 10 μF with ±1-pF accuracy. You can get a detailed schematic from "Capacitance meter uses PLL for high accuracy" on the *EDN* Website (Ref. 1).

The circuit generates two signals of the same frequency that are 60° apart in phase. A PLL (phase-locked loop) adjusts the frequency of its VCO (voltage-controlled output) to get the two signals in phase. With the signals in phase, the VCO's output frequency is 6 $F_0$, which is six times the frequency produced by the RC circuit containing the capacitor under test.

The meter has two ranges: 1 pF to 0.01 μF and 0.01 μF to 10 μF. When using the higher capacitance range, the meter's divide-by-1000 counter is in the circuit to reduce $F_0$ so that the VCO can attain a frequency lock.

The meter's circuit includes a divide-by-six counter in the VCO feedback loop that reduces the VCO's input signal to its original frequency. A divide-by-three counter reduces the VCO output frequency to 2 $F_0$. That signal can go to a frequency counter, which can display the unknown capacitance.

*Martin Rowe, Senior Technical Editor*

REFERENCE


1. McLucas, Jim, "Capacitance meter uses PLL for high accuracy," *EDN*, October 8, 2009. www.edn.com/designideas.



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# Test ideas

Measurement tips from readers

## Signal generator runs on Visual Basic

*Generate signals from 1 kHz to 68 MHz with two ICs and a few components.*

By William Grill, Riverhead Systems

Test applications often call for a clock signal. Rather than tie up a function generator, you can build a programmable clock generator with just two ICs. You can then control the clock generator with a Visual Basic application that handles frequency setting, provides interactive displays, and programs the circuit through the PC's serial port. (You can download the software from the online version of this article at www.tmworld.com/2009_12).

The clock generator circuit in **Figure 1** uses an LTC6904, a 1-kHz-to-68-MHz programmable oscillator (Ref. 1). It provides frequency accuracy of 1.1% over the full frequency span with sufficient supply voltage. A 9-V battery provides power for the circuit. A 78L05 linear regulator drops the battery voltage to 5 V, which powers the circuit. The circuit adds a Schmitt-trigger output buffer to isolate the LTC6904's output and increase current drive capacity from about 4 mA to 50 mA.

The LTC6904 uses a two-wire $I^2C$ protocol for its programming. The software interfaces the serial port to the LTC6904 using the RS-232 DTR (data terminal ready) and RTS (request to send) signals on connector pins 4 and 7, respectively. You can use the software to select the clock generator's output frequency and select the PC's serial port (1 through 6).

The LTC6904 is configured with 16 frequency blocks, each with resolution of 1024 steps. The knob at the lower left of the control window (**Figure 2**) loads the LTC6904 with 100 index steps while the right knob will index the output frequency by a single internal step.

When you change a knob setting, you'll see the new frequency in the numerical display. When you press the send button, the software will calculate the closest of the 16 frequency blocks and the index value. The code with then send the new frequency data to the LTC6904 through the serial port while displaying the frequency.

To calculate frequency, the software uses this equation:

$$frequency = 2^{OCT} \cdot \frac{2078\ \text{Hz}}{2 - \left(^{DAC}/_{1024}\right)}$$

where 1 kHz ≤ *frequency* ≤ 68 MHz. *OCT* is a four-bit code (0–15) that selects one of the 16 frequency blocks, and *DAC*

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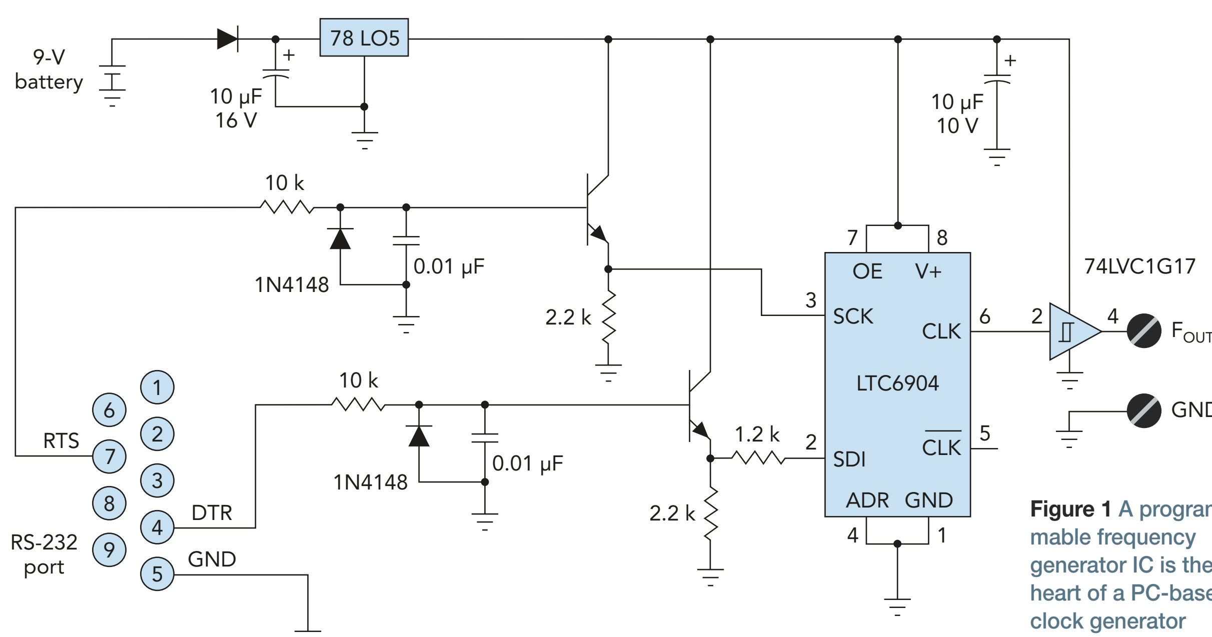


**Figure 1** A programmable frequency generator IC is the heart of a PC-based clock generator

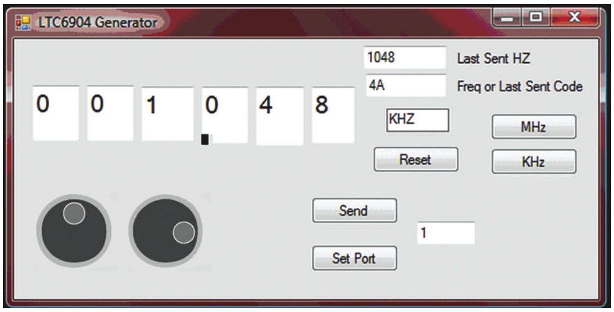


**Figure 2** A downloadable Visual Basic application lets you program the circuit's output frequency and select a serial port.

is a 10-bit code (0–1023) that selects the frequency within the selected block. The LTC6904 data sheet explains the programming in detail. T&MW

REFERENCES


1. "LTC6903/LTC6904 1kHz - 68MHz Serial Port Programmable Oscillator," Linear Technology. cds.linear.com/docs/Datasheet/69034fb.pdf.

2. "74LVC1G17 Single Schmitt-trigger buffer," Philips. www.datasheetcatalog.org/datasheet/philips/74LVC1G17GM.pdf.



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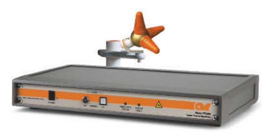

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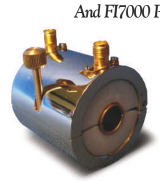

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*Test & Measurement World*'s editors have searched through many commendable products, nominated by vendors, that were introduced between November 1, 2008, and October 31, 2009. Now, it is up to you to help us choose the best of the best. On the following two pages, we present the finalists for the 2010 Best in Test awards. Visit www.tmworld.com/awards to cast your vote for your favorite product in each of the 17 categories. We will announce the category winners on April 1 at www.tmworld.com and in our April issue. In addition, the product that receives the most votes overall will be declared the 2010 Test Product of the Year.

We have also selected seven finalists for the Test of Time award, which honors a product that continues to provide state-of-the-art service five years or more after its introduction. Help us decide the 2010 Test of Time winner by casting your vote for the finalist of your choice. The Test of Time winner will also be announced April 1.

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TEST OF TIME

*OUR EDITORS HAVE SELECTED THE FINALISTS FOR THE BEST IN TEST AWARDS AND THE TEST OF TIME AWARD.*

BEST IN TEST

# BEST IN TEST 2010 FINALISTS

*Audio/video and multimedia*

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AUDIO PRECISION

**dScope Series IIIA Audio Test System**
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**MMTS Moving Video Test System**
VI TECHNOLOGY

**MVP-200 SimulTrackII Video Probe**
JDSU

**Netrounds Web-Based Network-Monitoring Tool**
ABSILION

**Sentry Digital Content Monitor**
MIXED SIGNALS

*Bit-error-rate testers*

**BERTScope CR 25000A**
SYNTHESYS RESEARCH

**J-BERT**
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**PCB12500**
CENTELLAX

**PeRT$^3$**
LECROY

*Board and system test*

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ASTRONICS DME

**Medalist i3070 Series 5 In-Circuit Tester**
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CONTEC

**SMART^E 5200 Satellite Payload Test Environment**
AEROFLEX TEST SOLUTIONS

**TS-720 GBATS Automated Test Platform**
GEOTEST—MARVIN TEST SYSTEMS

**URT 5.0 Universal Receiver Tester**
AVERNA

*Communications network test*

**iTest 3.4 Test Automation Software**
FANFARE

**K2 40Gb/100Gb Higher Speed Ethernet Load Modules**
IXIA

**T-BERD/MTS-4000 Multiple Services Test Platform**
JDSU

**TestCenter HyperMetrics 40/100G Ethernet Test Module**
SPIRENT COMMUNICATIONS

*Computer bus analyzers*

**Data Center 3.5 Software**
TOTAL PHASE

**Explorer 280 USB 3.0 Protocol Analyzer/Generator Duo**
ELLISYS

**PCIe Jammer Error-Injection Tool**
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LECROY

**Xgig Protocol Analysis and Test Platform for SAS and SATA**
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*Data acquisition*

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**Genesis HighSpeed GEN5i Recorder**
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**xDAP 7400 DAQ System**
MICROSTAR LABORATORIES

*DFT, boundary scan, and emulation*

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JTAG TECHNOLOGIES

**Juliet Desktop JTAG Tester**
GOEPEL ELECTRONIC

**kDiagnostics Software Platform**
KOZIO

**ScanWorks for Embedded Boundary Scan**
ASSET INTERTECH

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JDSU

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ANRITSU

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DALSA

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**SE500 Solder-Paste Inspection System**
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SVS-VISTEK

**Y.Cheetah X-Ray System**
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*Oscilloscopes*

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YOKOGAWA

**Infiniium 9000**
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**PicoScope 9211**
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*Semiconductor test*

**Cassini16 ATE System**
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*Wireless test (standard specific)*

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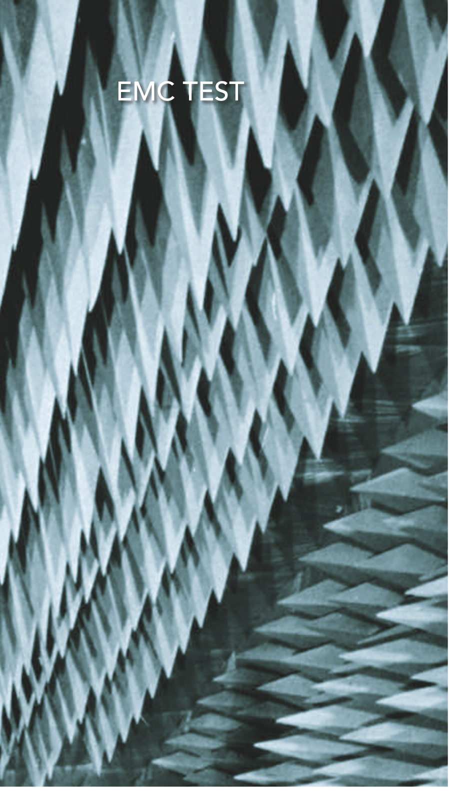

THE DESIGN, CONSTRUCTION, AND QUALIFICATION OF A CHAMBER DEPENDS ON THE PRODUCTS IT WILL TEST.

# ANECHOIC CHAMBERS *RISE FROM THE PITS*

BY MARTIN ROWE, SENIOR TECHNICAL EDITOR

Tests for electromagnetic immunity and emissions work best when located far from intentional transmitters such as broadcast stations and cell towers. Testing products for emissions or immunity in populated areas requires an anechoic or semianechoic chamber to keep ambient signals from interfering with measurements. Every chamber installation is unique and is influenced by many factors, some of which can change over time.

Major factors affecting chamber design include the size of the EUT (equipment under test), the relevant standards for EMC (electromagnetic compatibility), and the building facilities. A company that manufactures handheld devices won't need a chamber as large as one that makes rack-mounted equipment or vehicles. Chambers also differ depending on whether they must comply with commercial or military standards. Chambers used exclusively for emissions tests differ from those that also host immunity tests. Chambers used for precompliance tests and troubleshooting rather than full-compliance tests may also differ in size and construction from those used for full-compliance tests. ("What is an anechoic chamber?" p. 36, explains how chamber components minimize signals inside the room.)

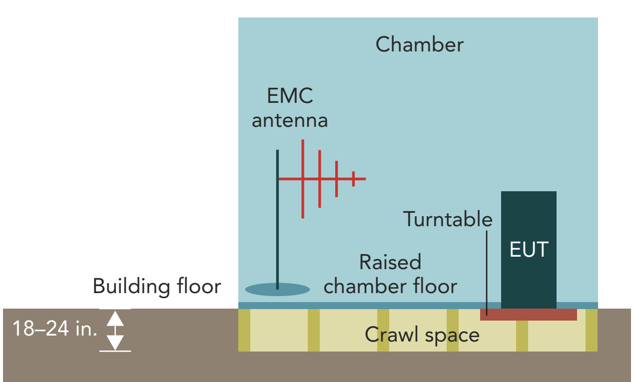


**FIGURE 1.** Many chambers sit inside a pit that provides space under the working floor.

## Know what goes in

Proper chamber design starts with a knowledge of the products that you need to test. "Have a good idea of your product roadmap over the next several years, because test requirements tend to grow over time," advised Bryan Sayler, Sr. VP and GM of ETS-Lindgren. Planning for future products eases decisions about a chamber's size, turntable size, cable routing, power provisioning, and instrumentation.

National and international EMC standards significantly influence chamber size, because they often specify the distance from the antenna to the EUT: 1 m, 3 m, or 10 m. For example, CISPR 22 requires a 10-m distance for EUTs larger than 2 $m^3$ (Ref. 1). Product size affects chamber size, because a chamber must be large enough to accommodate the distance from the EUT to the antenna, plus the size of the EUT, plus the size of any internal absorber materials. Absorbers such as cones that line a chamber's walls significantly reduce the usable area.

Chambers may also accommodate other distances such as 5 m. "Some test labs will use a 5-m distance for precompliance tests because it better correlates to how an EUT will perform at 10 m than a 3-m distance," noted Peggy Girard, president of Panashield. "Some chambers are designed to accommodate a 5-m path length, but currently the FCC will only accept the chamber based on the

3-m test data, because the agency doesn't formally recognize 5-m data in its comparison to an OATS (open-area test site).

The construction of the host building also affects chamber size, particularly height. When engineers at Northwest EMC opened a facility in June 2009 in Brooklyn Park, MN, they wanted a location close to potential customers, which ruled out an OATS. Operations manager Tim O'Shea explained that ceiling height was a critical factor, because many cities have building-height restrictions, and he needed a building with ceilings high enough to house a 10-m chamber, which can typically be 30 to 32 ft tall.

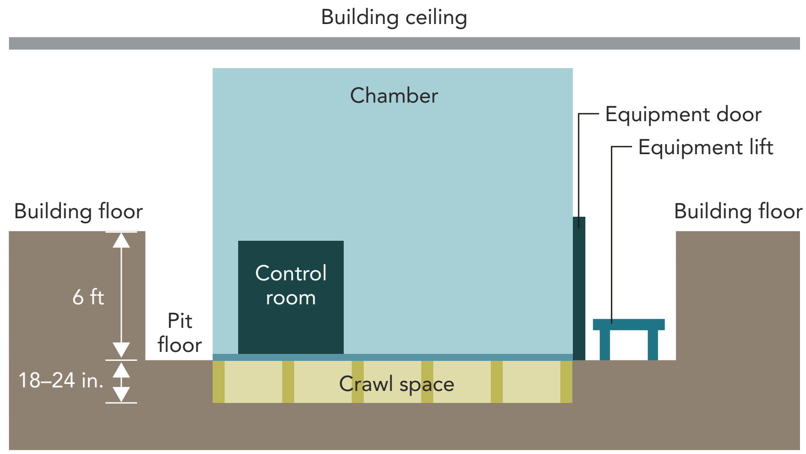


**FIGURE 2.** One chamber design needed a 6-ft pit to clear a building's ceiling.

## Rising from the pit

Height isn't the only consideration for a building to house an anechoic chamber. Depth counts, too. **Figure 1** shows a typical chamber with a raised working floor. The chamber floor is supported on legs because there's a pit under the floor. The pit, typically 18-in. to 24-in. deep, provides space for EUT support equipment and cable routing from the control room to the center of the floor's turntable. The raised floor is flush with the building floor outside the chamber, which lets technicians roll equipment into the chamber.

**FIGURE 3.** A chamber without a pit requires an equipment ramp. A swinging door lined only with ferrite tiles will clear the door opening. Courtesy of Panashield.

Girard described an unusual chamber that, because of low ceilings in the building that housed it, required a "pit within a pit." **Figure 2** shows that the chamber's raised floor was actually 6-ft below the building's floor. The 6-ft pit was larger than the chamber, providing working space outside the chamber at the chamber floor's level. A second pit extended 18 in. below the chamber's floor to provide space for cables and turntable motors.

Pits under chambers need not be as large as the entire chamber. To save on construction costs, some companies and test labs choose to leave much of the area under the chamber floor solid and just provide conduits for cables to the EUT, turntable, and antenna. While this design costs less to dig, it minimizes flexibility. Chambers with conduits also need metal pipes around the cables for electromagnetic shielding.

Instead of having just the 18-in. to 24-in. space under their raised floors, some chambers have deeper pits under the turntable or antenna. Ghery Pettit, EMC regulatory compliance manager at Intel, chose to construct a chamber with a 6-ft pit under the antenna. That depth provides space for RF amplifiers used in immunity tests. Keeping amplifiers close to an antenna results in shorter cables that carry RF signals. "We really wanted a 7-ft pit because 6-ft isn't deep enough for some people to stand. When we built a chamber in Dupont, WA, we dug a 7-ft pit so that anyone could stand upright in it."

Other chambers have no pits under them at all. Instead, the base of the chamber rests on the building floor, and the chamber has a raised floor under which the cables run. In that case, an equipment ramp (**Figure 3**) lets technicians roll equipment into the chamber.

Cables under a chamber floor provide power, control, and I/O signals to an EUT. RF cables connect antennas in the chamber to RF amplifiers for immunity tests or to EMI (electromagnetic interference) receivers and spectrum analyzers for emissions tests. Other cables provide power and control signals for turntables and antenna masts. Test equipment usually resides in a shielded control room close to the chamber.

## Connecting the cables

Because test equipment resides in a separate control room, all chambers need penetration panels that hold cable connectors. Cables on either side of the panels connect equipment in the control room to the EUT, turntable, and antenna inside the chamber. The control room should be located close to the portion of the chamber that holds the panels in order to minimize cable length.

For commercial EMC tests, cables that come from outside the chamber generally run under the floor. The penetration panels may be part of a chamber's walls, or they can be on the floor next to the chamber, provided there's space under the panel for cable runs. At Northwest

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EMC's Brooklyn Park facility, penetration panels are located in the chamber's wall (**Figure 4**) next to the control room, but below the raised-floor's surface. At Intertek's facility in Boxborough, MA, connector panels are located on the floor of the control room (**Figure 5**). Cables then run through the pit under the floor to the center of the turntable. The raised chamber floor has panels through which the antenna cables can emerge to reach the antenna and its mast.

For military tests, cables must run on the chamber floor, because that simulates actual use. In addition, EUTs need not rotate. So, Tom Arcati, engineering specialist at Dayton T. Brown, uses chambers without pits or turntables (**Figure 6**). That simplifies the chamber's design and makes it less expensive than chambers used for testing to commercial standards. The penetration panel is on the chamber wall, slightly above the floor. "MIL-STD 461 requires at least 10 m of cable between the antenna and EUT," said Arcati. "Power cables from the LISN [line impedance stabilization network] and the equipment must be at least 2 m long."

EUTs often need external AC or DC power, so a chamber must be wired to make power available. The AC or DC power that a chamber must support varies with how the chamber is used. Independent EMC test labs test a wide range of powered products and require more forms of power than chambers dedicated

**FIGURE 4.** A penetration panel sits below the building floor, providing access to cables that run under the chamber's raised floor. A pipe opening alongside the panel provides access for additional cables and hoses.
Courtesy of Northwest EMC.

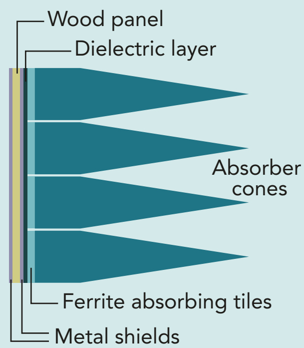
## What is an anechoic chamber?

Anechoic chambers perform two basic functions as part of an overall EMC measurement system. They shield a test setup from ambient signals, and they absorb reflected signals generated inside.

The walls and ceiling of a chamber are lined with metal that connects to a grounded metal floor, which serves as the ground plane required by many EMC standards. The metal lining, both inside and outside the walls, attenuates signals by providing a low-impedance path to the earth ground. A typical chamber can attenuate signals by at least 100 dB.

Unintentional emissions, radiated either by the EUT or by the signals intentionally transmitted from an antenna, will bounce off the shielded walls, creating undesirable fields inside the chamber. Thus, anechoic chambers need absorbing materials to minimize reflections.

The **figure** shows a typical wall construction. The wall consists of a wood panel sandwiched between two metal layers. The inside metal layer is lined with ferrite tiles and absorber cones typically referred to as hybrid absorber, which is impedance matched to the ferrite to allow for testing across the full range from 30 MHz to greater than 40 GHz.




**Chamber walls consist of shielding layers and absorbing materials.**

The ferrite tiles absorb signals up to about 1 GHz. If a chamber won't see higher frequencies, then it won't need the hybrid cones on top of the tiles. The cones, up to about 4 ft long, significantly reduce chamber size. They're typically made of carbon-loaded polyurethane foam, polystyrene foam, or fibrous material.

A chamber's raised floor is an integral part of the chamber's shielding and grounding. For radiated emissions tests, the floor—made of metal and often covered with vinyl—is grounded and is attached to the chamber walls. Radiated emissions standards such as ANSI C63.4 and CISPR 22 require a grounded metal floor that simulates signals bouncing off the ground of an outdoor facility. Because the floor isn't covered with absorbing materials, the chamber is called semi-anechoic rather than fully anechoic.

Radiated immunity standards such as EN 61000-4-3 require a partial floor coverage of absorbers between the front of the uniform field and the antenna for a 3-m path length, typically 10 ft wide by 11 ft long. Thus, absorbers must be on all six surfaces of the chamber. If a chamber is used for both commercial emissions and immunity tests, it will need removable absorbers for the floor.

Anechoic chambers used for commercial EMC emissions and immunity tests need a turntable that rotates the EUT, exposing all sides to an EMC antenna. EUT size and weight dictates the size of the turntable. Intel's Ghery Pettit has built three anechoic chambers in his career. The first, built in 1989 and still in use, has an 18-ft diameter turntable that can support 20,000 lbs.

Standards also require tests over different frequency ranges. ANSI C63.4 and CISPR 22 originally called for frequencies from 30 MHz to 1 GHz. CISPR 16-1-4 covers frequencies from 1 GHz to 6 GHz and up to 18 GHz. Military standards such as MIL-STD-461 call for conducted tests from 30 Hz to 80 MHz and for radiated tests from above 80 MHz to 40 GHz.

*Martin Rowe, Senior Technical Editor*

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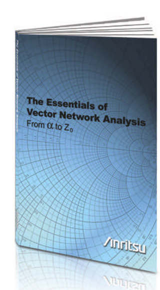


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*The Only High Performance VNA Designed and Manufactured in the USA* to one company. The type of power also depends on national compliance standards. For example, a chamber might need 100 V for Japan, 110 V for Taiwan, 120 V for North America, and 220 V for Europe. It may need to provide power frequencies of 50 Hz, 60 Hz, or 440 Hz, single phase or three phase.

The AC mains lines that enter a chamber require filtering to minimize noise. Some chambers filter their AC voltages using a single filter for each voltage, then distribute the clean power to the equipment inside the chamber. Some EMC engineers, however, prefer to distribute the power to its load and filter it there. The choice depends on cost versus flexibility.

Because power and signal cables must connect to an EUT on a turntable, the cables must have enough slack to accommodate turntable rotations. "Most turntables have 380° of rotation," said Sayler of ETS-Lindgren. "The turntable typically rotates ±180° during a test." A more expensive approach, and one that he rarely sees, uses slip rings that conduct power and signals while permitting continuous rotation.

## Designing the doors

Regardless of whether a chamber is used for commercial or military tests, it needs a door large enough to get an EUT in and out. The size and design of a door also depends on the products tested in the chamber. Size and location are important. Intel's Pettit noted that "The door locations should minimize the distance to the turntable if the chamber will test large, heavy EUTs."

Door location matters for more than just convenience. Sayler warned that "There are electrically good and bad places for chamber doors. If the door lacks cones, it should be as far away from the turntable as possible because it will affect the quiet zone around the turntable."

Engineers at Northwest EMC use their chamber for radiated emissions only, and the EUTs are typically small enough to fit on a table. Thus, the chamber has two 4-ft by 8-ft swinging doors for equipment entry and exit. The inside of the doors don't have absorbing cones because they would interfere with the door opening in the chamber wall. The door has ferrite tiles lining its inside surface. Figure 3 shows a single door lined with ferrite tiles, but no cones, so the door can clear the door opening. In contrast, the chamber at Intertek's Boxborough facility has a retractable door, and thus has cones, but costs considerably more than a swinging door. Swinging door leaves can have cones over the ferrites provided the cones can clear the door opening (Ref. 2).

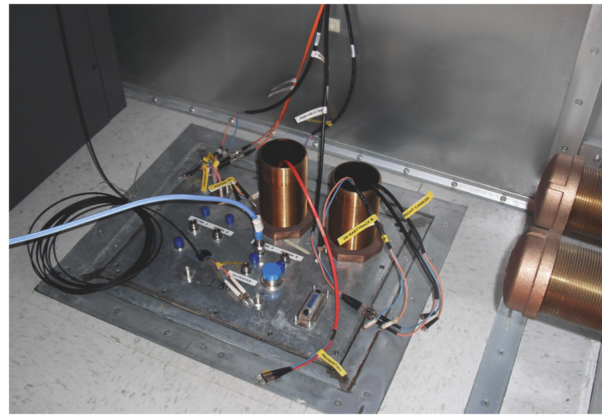

**FIGURE 5. A floor-mounted panel provides power and signal cables with access to the inside of a chamber.** Courtesy of Intertek.

## Qualifying a chamber

Because anechoic chambers are shielded rooms, they must prove that they sufficiently attenuate outside signals before a manufacturer installs internal absorbers. Most EMC engineers specify that chambers attenuate outside signals by at least 100 dB. "We can build chambers that attenuate up to 120 dB for areas high in ambient signals," said Sayler. "For most applications, 80 dB of attenuation is enough." Remember that it is the ambient noise levels inside the chamber that count. If a chamber is in a region of relatively low ambient signals, then 80 dB of attenuation may be sufficient.

A technician will test the chamber's shielding effectiveness by generating a signal at a known power and frequency and measuring signal strength on the other side of the wall. O'Shea explained the test procedure at Northwest EMC. "We had the transmit antenna at 26 different locations outside of the room—including the top—and moved the receive antenna along all inside seams closest to the transmit position. We checked every seam in the room."

Technicians may also perform shielding-effectiveness tests with the transmit antenna outside the chamber and the receive antenna inside. Placing the receive antenna in the chamber reduces ambient signals at the receiver, which makes the transmitted signals easier to see on a spectrum analyzer.

Following a shielding-effectiveness test, a chamber is ready for the absorbing materials. After installation, the chamber needs additional measurements around the turntable to verify its quiet zone for radiated emissions tests per IEEE C63.4 from 30 MHz to 1 GHz (Ref. 3) and per CISPR 16-1-4 (Ref. 4). For

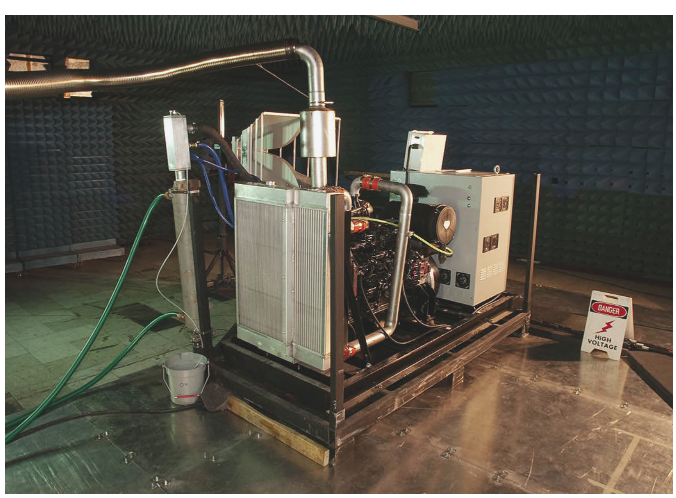


**FIGURE 6. Chambers designed for MIL-STD-461 compliance tests don't need turntables; cables for these tests can run on the chamber floor.** Courtesy of Dayton T. Brown.


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radiated immunity tests, a chamber must undergo a field-uniformity test to comply with EN 61000-4-3 (Ref. 5).

**Do this, not that**

The engineers I interviewed for this article offered some tips for building an anechoic chamber. Panashield's Girard urged an understanding of your needs. "Start by knowing what your present and future testing needs will be for your product, per international standards. Will you require radiated emissions, immunity, or both?"

O'Shea of Northwest EMC said, "Plan ahead. Look at the whole facility and how the chambers will fit into the building. Evaluate customer needs to customize room size, turntable size, door size, power requirements, etc. Don't take shortcuts in the building process or during shielding effectiveness testing because this could cause problems that are much more difficult to fix once the room is fully constructed."

Sayler of ETS-Lindgren added, "Get on the good side of your facilities people. You'll need them."

And Intel's Pettit expressed concern for AC mains power. "Have plenty of power, at least 100-A service for each voltage. Separate power feeds from the turntable to the EUT so you won't get interference." T&MW

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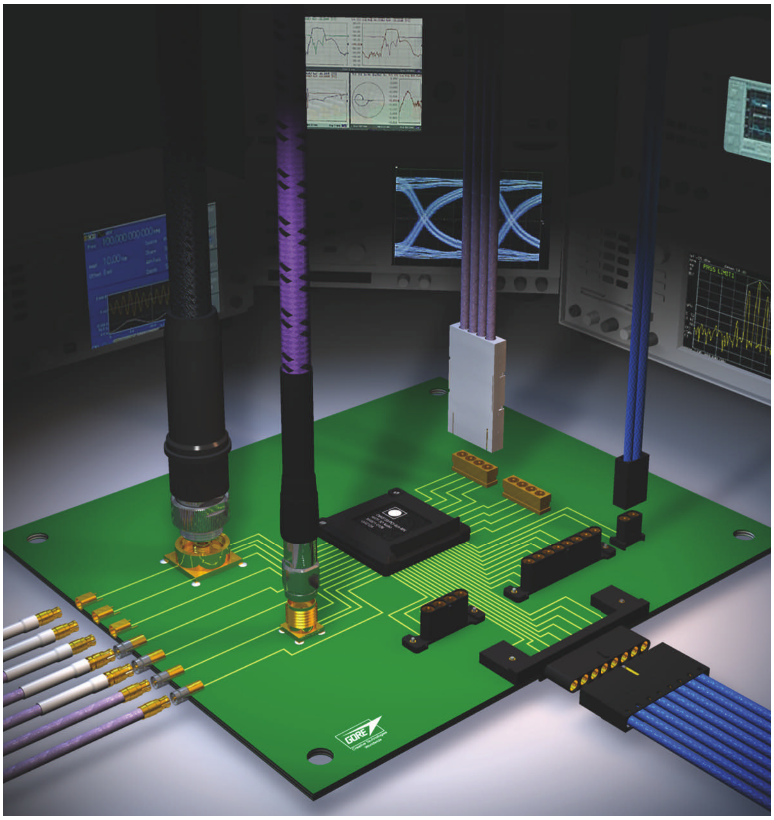


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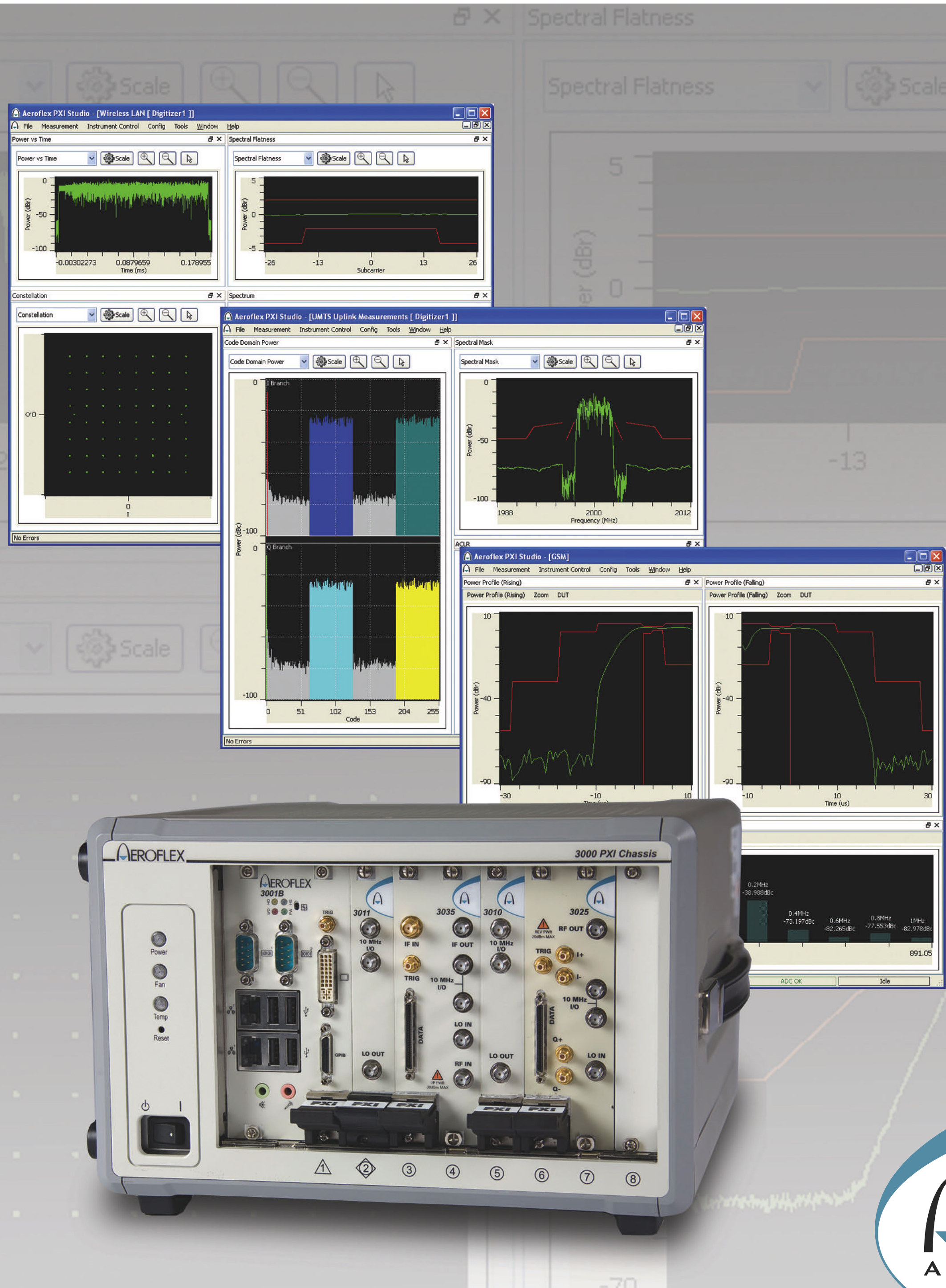


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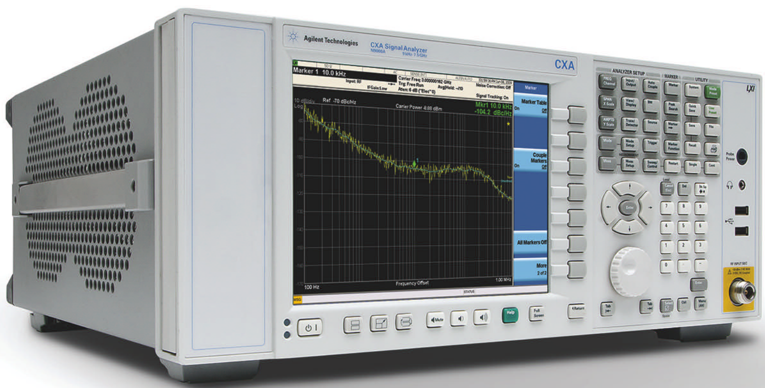


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# The changing role of DIAGNOSIS *in* YIELD ANALYSIS

**An infrastructure that captures and automatically diagnoses each manufacturing test failure can accelerate yield analysis.**

BY GEIR EIDE, MENTOR GRAPHICS, AND DAVIDE APPELLO, STMICROELECTRONICS AUTOMOTIVE PRODUCT GROUP

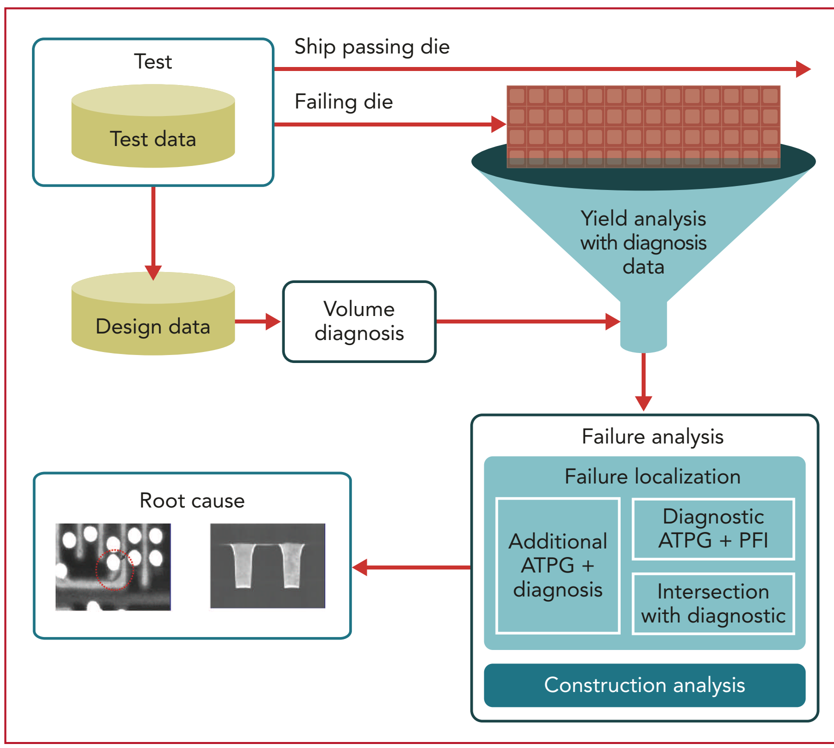


**FIGURE 1. A diagnosis-driven yield-analysis flow can increase your chances of picking the right die for failure analysis. The failure-localization step, which includes diagnostic automatic test-pattern generation and physical-fault isolation, is optional.**

Test-failure data contains a wealth of information that can accelerate the yield-analysis process for semiconductor devices. By setting up an infrastructure that captures and automatically diagnoses each manufacturing test failure, you can create a valuable database of information based on actual silicon results. When you couple this database with a diagnosis-driven yield-analysis tool that performs statistical analysis on this large volume of diagnosis data, you can significantly reduce the time needed to recognize systematic yield issues and determine their root causes.

## The role of scan diagnosis

A key goal in the yield-analysis process is to identify the root cause of yield loss. The most significant challenges include

- separating devices with systematic issues from those with random defects,
- identifying fail-mode similarities across multiple failing die, and
- localizing and identifying physical defects.

Scan diagnosis is an established software-based method for defect localization and is used as part of the failure-analysis process (see "Yield challenges and traditional tools for semiconductor companies," p. 45). Scan diagnosis identifies the location and classification of a defect on a die based on the design description, the test patterns used to detect the failure, and the failure data from the tester. A scan-diagnosis tool will typically process each failing die individually. For each defect on each die, the diagnosis tool will output a list of "suspects;" that is, suspected defect locations and mechanisms.

The quality of a diagnosis result is typically measured by accuracy and resolution. A diagnosis result is accurate if the actual defect location is in the list of suspects that the diagnosis tool generates. The resolution of the result is determined by the number of suspects in the list and by the physical area where the suspects reside. For instance, the tool may provide a suspect list of 10 nets, while the actual defect affects just one of these 10. A higher resolution tool would provide only one net or, even better, just a segment of the net where the actual defect is located.

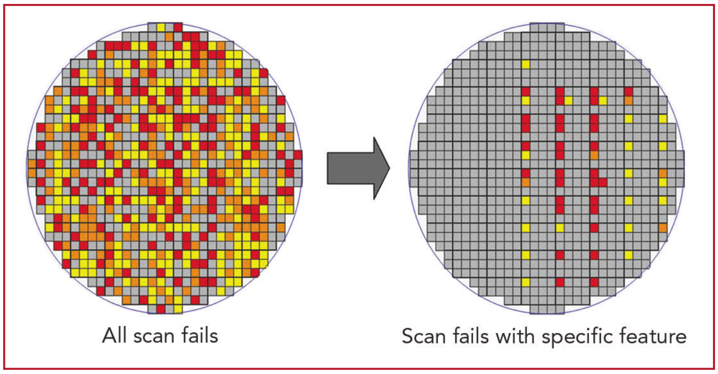


**FIGURE 2.** (left) A visible pattern may not be evident from a stacked wafer map of all failing die, but you can use zonal analysis to separate systematic defects from random issues. (right) Die corresponding to the upper left corner of the reticle failed systematically.

### Extending the role of diagnosis

To address the first two challenges listed above—separating devices exhibiting systematic issues from those with random defects, and identifying fail-mode similarities across multiple failing die—you must select the right devices for failure analysis. This selection has traditionally been done without the aid of diagnosis, and it may be a trivial task if the presence of a systematic issue is obvious. For example, if all but one wafer has zero defects, and this one wafer has 100 failing die that are all in the center of the wafer, you can assume with relative certainty that all these die fail for the same reason. No matter which die you pick for failure analysis, the die will represent the root cause.

But at very small process nodes, a combination of effects can easily mask systematic issues and produce failure patterns on a wafer map that appear random. In these situations, you need tools that examine diagnosis data from large numbers of die in order to recognize patterns in the data that point to systematic causes. Such diagnosis-driven yield-analysis tools use statistical techniques to recognize correlations based on many different factors, helping to point you to views of the data that have meaningful information.

Consider a hypothetical example where most wafers have 50 failing die, but one wafer has 100 failing die. If you randomly pick one die for failure analysis from the excursion wafer, you have only a 50:50 chance that the selected die has a defect related to the increased fall-out on that particular wafer. In other words, it can be hard to distinguish between systematic and random issues, especially if multiple systematic issues are hidden in the data. Chances are that when selecting devices for failure analysis, you will end up with devices that failed for different reasons.

To increase your chances of picking the right die for failure analysis, you can use scan diagnosis to look for patterns across a large number of failed die by integrating a volume diagnosis step into your testing and yield-analysis process (**Figure 1**). In a traditional flow, scan diagnosis is not used until the physical-failure-localization step, which is done before construction analysis. In a diagnosis-driven yield-analysis flow, you can employ scan diagnosis earlier to help select the correct die and thus eliminate the costly physical-failure localization step.

The diagnosis-driven yield-analysis tool will classify the results of the scan diagnosis into categories such as defect mechanism, cell type, logic, and physical locations. This classification step enables you to separate the die into correlating categories such as defects in different instantiations of a particular standard cell or defects involving a particular type of via.

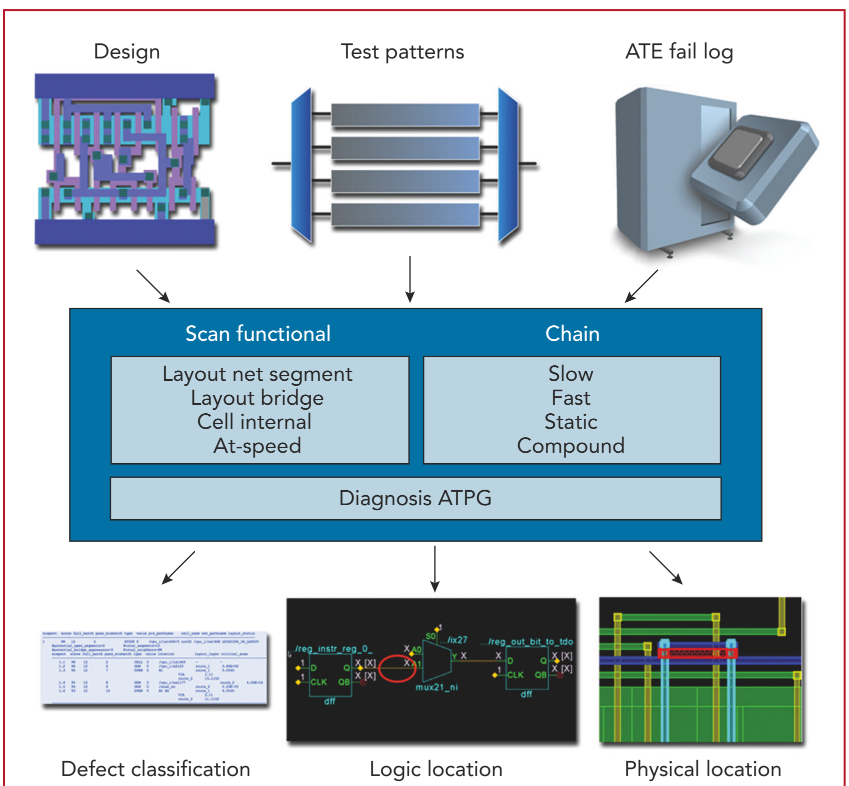


**FIGURE 3.** Scan diagnosis as performed by the Mentor Graphics Tessent Diagnosis tool makes use of design, test-pattern, and ATE fail-log input data; the tool then outputs defect classification, logic location, and physical location.

### Effectively using volume diagnosis results

What ultimately determines the value of diagnosis in yield analysis is how the diagnosis results are used. To effectively leverage diagnosis results, you need to separate systematic issues from noise (Refs. 1, 2, 3). You can approach this in several ways.

In the case of a typical yield excursion, yield loss is easily observable. To get to the root cause in such a case, you would group devices with common failure features and then select those devices with the most representative, highest-resolution diagnosis results for failure analysis.

For example, consider the hypothetical case of an excursion wafer that has 250 failing devices, 150 with suspected bridge defects. Of these 150 die, 120 have bridges in the metal2 layer. Of the 120, there are 50 with just a single diagnosis suspect, and out of this subset, 20 have high-resolution results. By leveraging diagnosis data in this way, you can find the suspected systematic defect mechanism (bridge in metal2) before failure analysis and select a device that clearly exhibits this behavior. Then, you can skip the costly physical-localization step and go straight to construction analysis.

In other cases, when multiple issues are present, separating random from systematic issues may be challenging. When you look at a stacked wafer map of all failing die, a visible pattern might not be evident, as shown in the left wafer map in **Figure 2**. To determine the presence of systematic failures, you could randomly select a large number of devices for diagnosis and failure analysis and hope that many would exhibit the same failure. This approach is costly and time-consuming. *(continued)*

## Yield challenges and traditional tools for semiconductor companies

Yield challenges for semiconductor companies vary based on many factors. As manufacturing ramps up for a product, yield loss is often clearly observable, and the challenge is to rapidly identify the root cause. Once the most severe issues are resolved, subpar yield may still be observable, but identifying which devices are failing because of systematic versus random issues becomes even more challenging. Once yield has reached mature levels, hidden systematic yield loss can go unnoticed, causing lower than optimum yield and higher DPPM (defective-parts-per-million) levels.

Which particular yield challenge is most important to a semiconductor manufacturer depends on the type of company, product type, device size, process node, and target market. Time-to-volume is a critical concern for manufacturers that create products with very short life cycles, such as advanced graphics chips. Increasing mature yield is typically of interest to IDMs (integrated device manufacturers) and foundries, while a fabless semiconductor company may or may not be concerned, based on whether it pays for tested or untested wafers.

Another important reason for analyzing mature yield is to improve product quality, which is measured in shipped DPPM. A defect mechanism that contributes to a very small portion of the overall yield loss may still contribute to a large proportion of the DPPM if it's a defect mechanism that isn't effectively screened.

While DFM (design for manufacturing) and DFY (design for yield) techniques can help ensure that designs are manufacturing friendly, an additional methodology can be used to analyze the actual fall-out based on silicon testing—diagnosis-driven yield analysis. Although this technique is a stand-alone solution, it can also be used to correlate actual failures with DFM violations to help prioritize verification rules.

### Traditional scan-diagnosis tools

Traditionally, scan-diagnosis tools relied on the stuck-at fault model and could diagnose down to a logic net. Although this approach is useful for localization, it has some limitations. Stuck-at patterns typically detect a vast variety of defect types, including bridges and opens, but this model is not always sufficient for effective diagnosis. Even a single suspect net could cover a large area of the die.

Over the last few years, these limitations have been addressed through technologies such as layout-aware diagnosis (Ref. 1), cell-internal diagnosis (Ref. 2), scan-chain diagnosis (Ref. 3), and at-speed diagnosis (Ref. 4). Advanced tools can diagnose defects down to a logic net and physical polygon, and they can differentiate between defects internal to the cells versus defects in the interconnect. Newer tools can also accurately classify a wide range of defect types. In addition, iterative diagnosis can increase the initial diagnosis resolution (Ref. 5). Diagnosis can now be used in conjunction with scan-test-pattern compression (Ref. 6) and logic built-in-self-test (Ref. 7). These advances have significantly improved the value of diagnosis for failure analysis and have also paved the way for using scan diagnosis in other areas.—*Geir Eide and Davide Appello*

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A different approach involves diagnosis followed by identification of the most variant failure features. For instance, while the distribution of failing die may appear to be random, the distribution of die with one particular diagnosis signature, such as devices failing for one particular type of standard cell, may be systematic in nature; as shown in the right wafer map in Figure 2. The pattern shown in this example indicates that the die representing the upper left corner of the reticle failed systematically. This information is useful in determining the root cause.

The technique used here is called "zonal analysis" and is used in the Tessent YieldInsight tool from Mentor Graphics (**Figure 3**). It is one of many possible correlation techniques. With zonal analysis, the tool automatically examines the various diagnosis signatures of many failing die and flags those that have an unexpected distribution across the data set. Another technique is to correlate failures with DFM (design for manufacturing) violations. No matter which cross-correlation technique is used, the intent is to separate the valuable results from the noise.

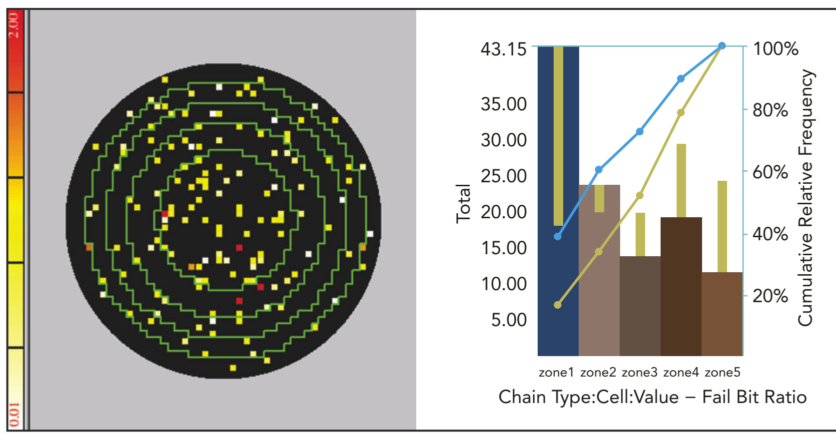



**FIGURE 4.** Center-border fail-distribution data illustrated deterioration in performance moving from wafer border (zone 5) to center (zone 1).

### Practical requirements for volume scan diagnosis

To use a diagnosis-driven yield-analysis flow, you need to manage the process of collecting failure data from multiple test systems and automatically performing volume scan diagnosis. One factor that makes this challenging is that different ATE (automated test equipment) platforms have different capabilities in terms of how much data they collect and how well they collect it. Besides this, two other factors complicate the collection of logic test failures: the lack of data-log format standards, and the lack of ATE operating system features that support failure-log data collection.

Consequently, to be able to implement volume scan diagnosis, you have to ensure that failures are correctly logged with robust data-traceability features. And you'll want to do this in a way that minimizes the impact on test quality, test throughput, and tester and computational resources.

Most semiconductor companies use a combination of stuck-at and at-speed test patterns. The majority of defects may fail both of these pattern sets, but diagnosing at-speed patterns requires more effort, because they are typically more complex and longer than stuck-at patterns. In addition, one particular defect mechanism may cause failures in the functional circuitry for some devices and in the scan chains themselves for other devices, but diagnosing scan-chain defects requires significantly more data than diagnosing failures in the functional circuitry.

In general, the more fail data that is collected, whether scan or functional, the better the diagnosis result. You can still perform an effective diagnosis with a relatively small amount of fail data per die. This is important, because in many cases, it is not practical to collect data from and perform diagnosis on all failing die. The minimum number of die needed depends on the type of issue to be analyzed.

For instance, the analysis of an excursion has different requirements compared to identification of a hidden yield limiter. As a sample calculation, assume a known systematic signature has been responsible for 5% of yield loss. To have a statistically significant sample, you may need at least 25 die that have this signature. Thus, data will be needed to be collected on 500 die (that is, 25 divided by 0.05).

### Example application of diagnosis-driven yield analysis

Diagnosis-driven yield analysis is particularly relevant during two situations: a new technology introduction, and a new product introduction. In both cases, critical issues affecting yield are common. You may need to simultaneously explore multiple sources of the root cause of failures.

At STMicroelectronics, we dealt with a scenario that combined both a new process technology and a new product. Since the early maturity phases, both the yield data for the TC (test chip) and the yield and diagnosis information for the final product, an SOC (system on chip), were available. The yield of the TC and SOC were different despite the designs being comparable in size. A possible explanation for the difference resided in the different architectural and topological complexity of the two designs.

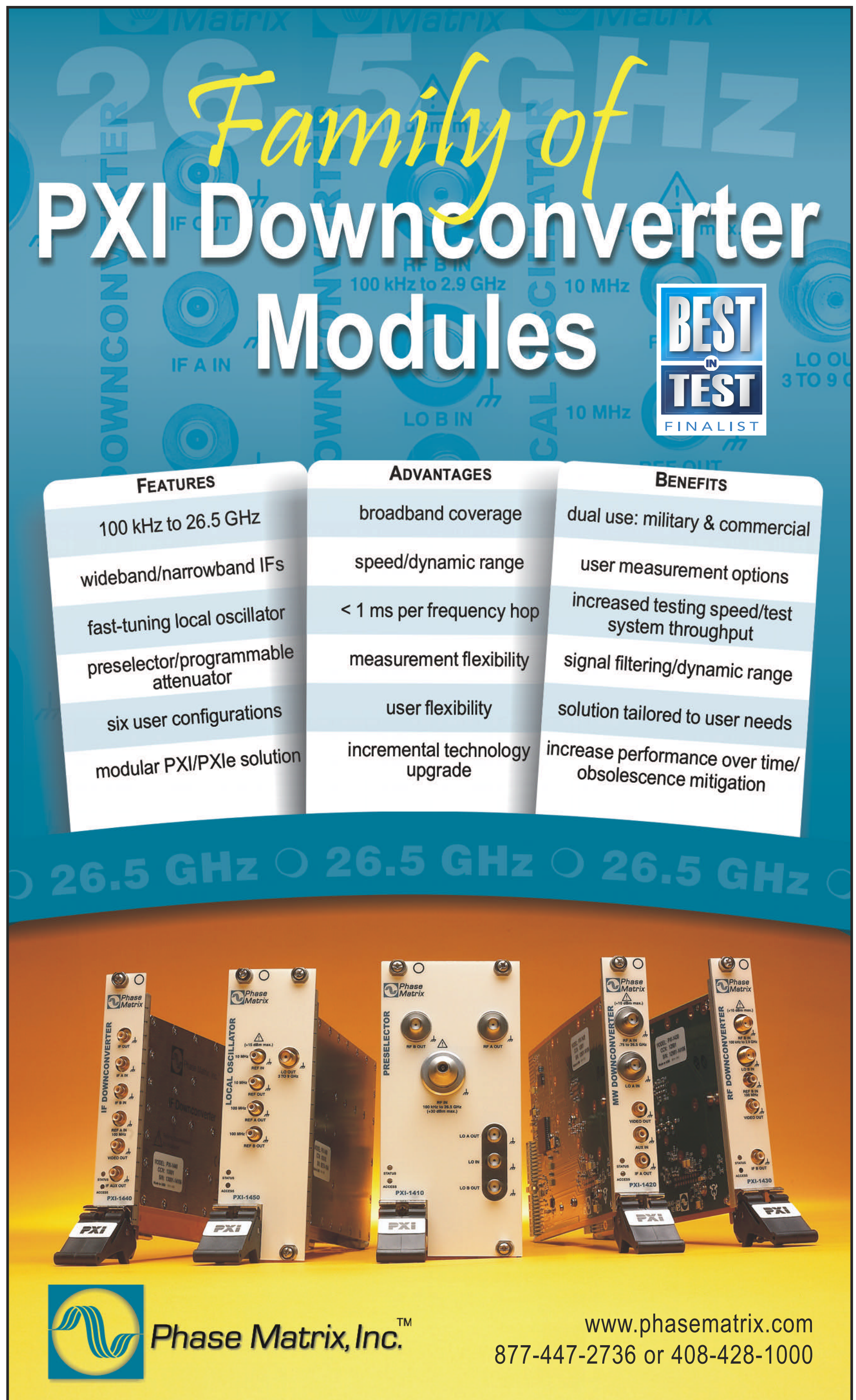
TCs are designed to explore yield performances of different layout configurations and to validate IP libraries. They typically have regular structures such as RAM and ROM or cell arrays. They also include ring oscillators and arrays of combinatorial and sequential logic cells. Electrical activation is made as simple as possible to reduce the variables that would have to be considered during the analysis of the test results.

On the other hand, end-product SOCs are irregular structures, in which the electrical activation complexity depends on many factors driven by functional requirements. The structural differences between TCs and SOC products with respect to electrical activation provide critical information that can be applied to yield analysis.

In the early phases of a new technology introduction, several defect sources may be aliasing each other. The observed failures may therefore indicate a different defect mechanism than those actually causing the failures. This was exactly the case we faced with the yield gap that existed between the STMicroelectronics TC and SOC products.

The first analysis action we took was to verify if and how the yield was affected by any type of systematic marginality that was dependent on the SOC implementation. The dependencies could have been timing-critical paths, crosstalk effects between adjacent wires, or power limitations. We used volume scan diagnosis to help verify design-related systematic effects.

We expected that the failure signature would also include evidence of the prob-

lem. The simple cumulative analysis of the failure signature could indicate the presence of the systematic problem, and the cumulative analysis of the diagnosis results would allow us to find the fault location with a better resolution.

In our case, no symptoms were present that indicated design issues. Consequently, we proceeded to filter out from the diagnosis results all signatures of a random nature. To do this, we used the TC information as well as comparative analysis across multiple sets of material.

For our second step, we employed zonal-analysis techniques to isolate the signatures that were present. We observed two combined factors: a deterioration of performance moving from wafer border to center (**Figure 4**), and a similar, emphasized behavior exhibited by some core library cells. By analyzing the layout of the library cells that exhibited the deteriorated performance, we were able to determine whether the defects occurred in the same relative location and to guess the possible criticalities associated with them.

The third step was to select a few die across the many that showed a similar signature, where confidence on symptoms was higher. In addition to the die

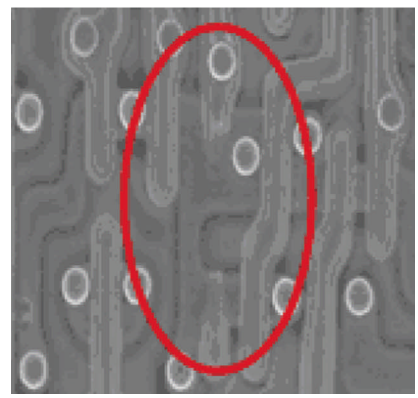


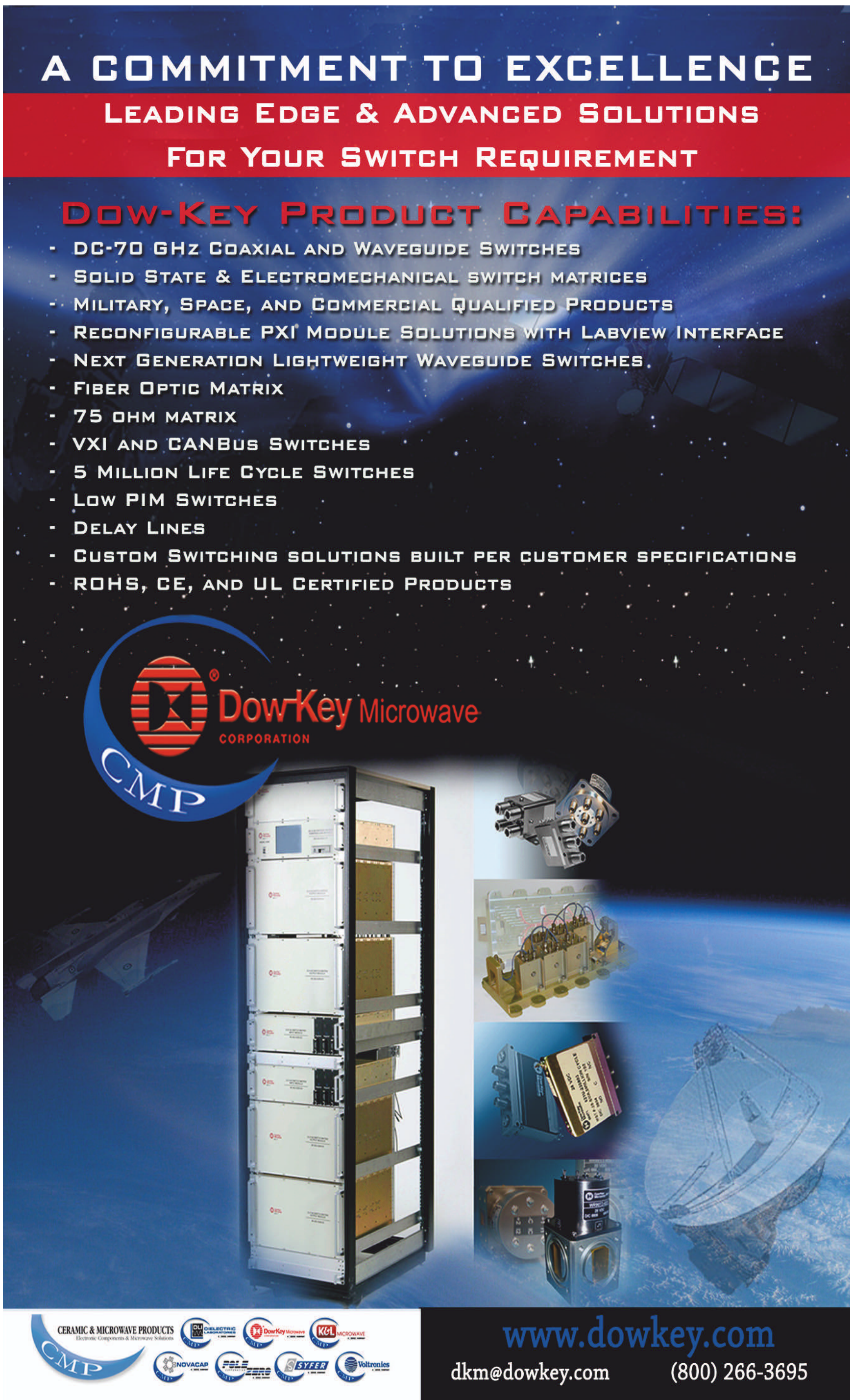
**FIGURE 5.** A poly-open defect found in one failing die classified as not affected by systematic fail mode confirmed the presence of physical defects not exhibiting a systematic nature.

exhibiting the systematic issue, we also selected die that were classified as affected by a random defect in order to confirm the presence of physical defects not of a systematic nature (**Figure 5**). Our physical analysis confirmed that the marginality on performance was caused by an improper process centering.

The fourth and final step, in parallel to tuning the manufacturing process, was to continue to observe the failure signature trend. This was done to verify that the critical signature was becoming negligible as a result of the process tuning.

## Where does diagnosis-driven yield analysis fit?

A yield-analysis flow based on scan diagnosis is not meant to replace all the other yield-improvement techniques that are in use. Rather, it supplements established techniques. A yield-management system continuously monitors data from multi-



ple sources and provides a high-level view, quickly informing if something is going awry.

Diagnosis-driven yield analysis involves deeply diving into both the design and test failure data of the specific device, rather than only relying on manufacturing process data. Consequently, it can often provide more specific information to guide the physical failure-analysis step, and it can help uncover design-related systematic issues that are difficult to discover using process data alone.

Diagnosis data collected in volume can also be exploited for monitoring purposes, as a shift in the process performances may lead to a variation in the electrical signature. Thus, diagnosis should be added to the other traditional instruments used for yield analysis to reveal the effect that defects have on the electrical behavior of the SOC.

While yield analysis has traditionally been an issue for IDMs (integrated device manufacturers) and foundries, sometimes fabless semiconductor companies need the ability to analyze yield. A diagnosis-driven approach may be suitable in these cases, because the focus is on test results rather than manufacturing results.

Diagnosis-driven yield analysis can also be used to improve the effectiveness of DFM rules by correlating actual root causes to rules employed during verification and setting higher priorities for those rules that would mitigate the types of failures experienced. In this way, design sensitivities are uncovered to drive yield learning across many designs at a particular process node. This is also important in a foundry environment where many designs may be sharing the same manufacturing line. T&MW

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**Geir Eide** *is a product marketing manager for the Silicon Test Solutions group at Mentor Graphics, where he has also held positions as development engineering manager and technical marketing engineer. Previously, Eide held an applications management position at Teseda. He earned a BS and an MS in electrical and computer engineering from UC Santa Barbara.*

**Davide Appello** *is silicon validation and test engineering manager at STMicroelectronics Automotive Product Group. Previously, he held several positions at STMicroelectronics in test development and product industrialization. He earned a degree in electronic engineering from Universita' di Pavia in Italy.*



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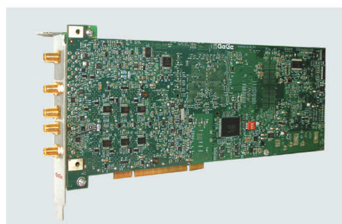

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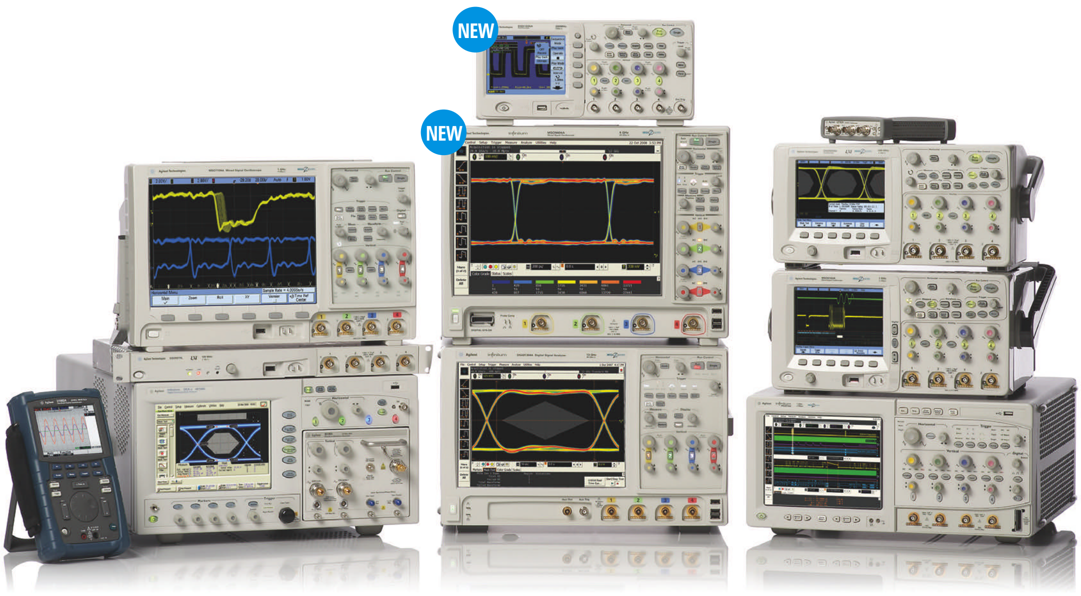


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# ATE facilitates WiMAX RF test and characterization

**For proper WiMAX transceiver device testing, an RF semiconductor tester needs to test accurately and quickly and also assist in device characterization.**

BY RON WALTMAN, ANALOG DEVICES, AND PETER HIGGINS, TERADYNE

WiMAX transceiver devices have proven to be a boon to the consumer electronics market, where they have found multiple uses including connecting a WiFi hotspot to the Internet. To ensure the devices work as promised and to bring them to market quickly, device manufactures need sophisticated, multifunctional test equipment and equally sophisticated test software.

## WiMAX capabilities

WiMAX is an RF technology developed to provide "last mile" broadband access as an alternative to wired DSL or cable. Based on the IEEE 802.16 standard, WiMAX technology has a range of a few kilometers, compared to the tens or hundreds of meters that WiFi (IEEE 802.11) offers.

Popularly adopted WiMAX carrier frequencies include 2.3 GHz, 2.5 GHz, and 3.5 GHz with channel bandwidths of 3.5 MHz, 5 MHz, 7 MHz, and 10 MHz. Like other digital modulation schemes, WiMAX provides longer transmission paths using a simpler modulation scheme with reduced data rates. If the path length is short, complex modulation schemes provide high data rates with low bit-error rates. To achieve high data transmission rates, WiMAX devices use numerous channels of MIMO (multiple input, multiple output) technology.

The "sister" version of WiMAX is WiBro (Wireless Broadband), developed by the South Korean telecom industry. Also known as mobile WiMAX and incorporated into IEEE 802.16e, the technology has a slightly different frequency band allocation around 2.3 GHz.

WiMAX uses OFDM (orthogonal frequency division multiplexing), a multiplexing technique that subdivides the bandwidth into multiple frequency subcarriers. In an OFDM system, the input data stream is divided into several parallel substreams of reduced data rate, and each substream is modulated and transmitted on a separate orthogonal subcarrier. In a 10-MHz channel bandwidth, data rates up to 63 Mbps are possible on the downlink between the base

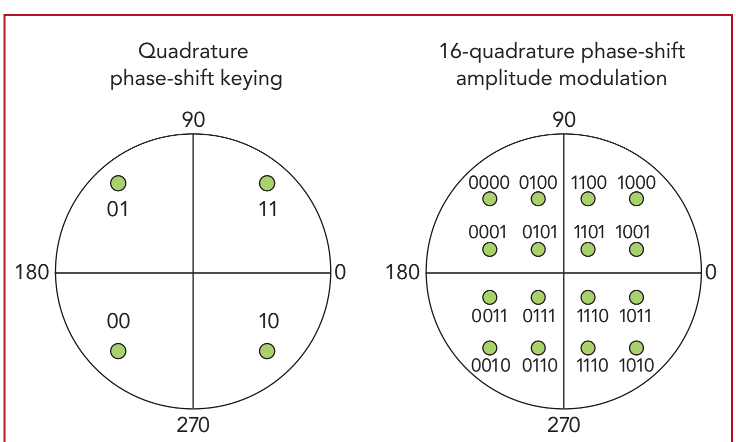



**FIGURE 1.** WiMAX modulation schemes include quadrature phase-shift keying and 16-quadrature phase-shift amplitude modulation.

ISTOCKPHOTO IMAGES

station and mobile unit, and rates up to 28 Mbps are possible on the uplink (**Figure 1**).

In early mobile devices, in-phase (I) and quadrature (Q) information would pass from the baseband processor to the RF portion of the device in analog format. In today's highly integrated devices, the ADCs and DACs reside in the same package as the RF circuitry, making the link between the RF device and the digital baseband processor a digital data bus. Moving the ADCs and DACs out of the baseband processor and into the RF device allows the processor to be fabricated on the smallest lithography possible, which reduces BOM (bill of materials) costs. **Figure 2** shows the layout of a typical RF MIMO transceiver with digital interfaces and multiple RF ports.

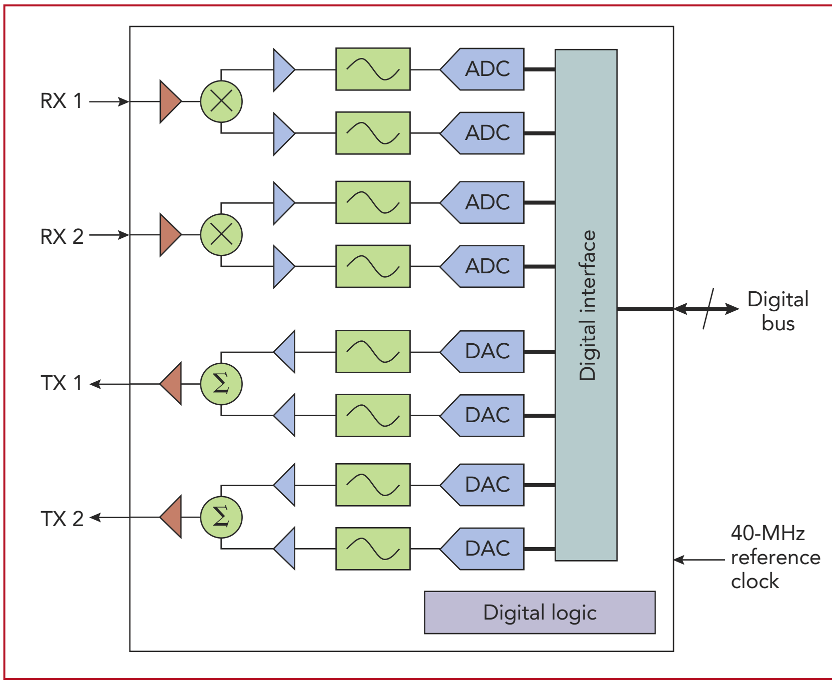



**FIGURE 2.** This WiMAX 2x2 MIMO transceiver block diagram illustrates a typical RF MIMO transceiver with digital interfaces and multiple RF ports.

## Requirements for WiMAX test systems

To test WiMAX transceivers on a high-throughput manufacturing line, an ATE (automated test equipment) system needs these key capabilities:

- digital sourcing and capturing at the same speed as the DUT (device under test),
- a low-phase-noise clock to provide a reference for the synthesizer,
- clean power supplies and ancillary control circuitry for relay control,
- RF sourcing and capturing,
- multiple RF ports that can be easily calibrated for accurate signal level, and
- methods of sourcing and capturing WiMAX modulated signals.

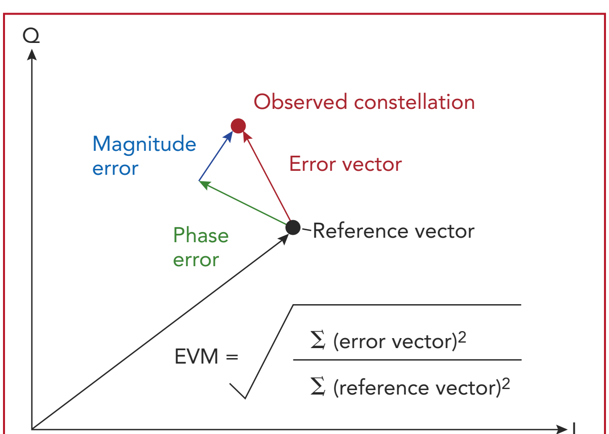



**FIGURE 3.** An EVM calculation indicates the difference between reference and observed points on a constellation diagram due to phase and magnitude errors.

The ATE system also needs to have enough resources—both hardware and software—to perform multisite testing with a high degree of parallel capability. Using parallel testing, the system should be able to test several devices in an overall test time that is close to what a single-site system would need to test one device.

During test development, you should align the tester resources in a way that minimizes the complexity of the load board. This allows the calibration of the RF signal levels to the tester delivery plane to be automatic from the test engineer's perspective. Just as devices should be designed to minimize the number of components on the PCB of the final assembled product, and thus lower the BOM cost, ATE load boards should also have as few components as possible. A "clean" load board with minimal components requires less time to design, lay out, build, and debug, and also proves to be more reliable in a volume production situation.

To test MIMO devices, the tester needs to provide multiple receivers to capture the devices' TX signals in parallel. It passes the captured waveforms to a modulation-analysis package that can interface with multiple input streams and analyze the combined information. The same process applies to the receive path, where multiple digital capture engines need to concurrently capture the digital data output of the devices' receivers.

A 2x2 MIMO device has two input RX and two output TX RF ports. For such a device to be tested in a quad-site arrangement, the tester must provide eight RF source and eight RF capture channels. To avoid splitters or RF switches on the DIB (device interface board), the ATE needs to provide 16 RF ports.

A quad-site application requires four high-purity reference clock inputs, one for each DUT's synthesizer. Low-phase noise of the clock inputs is paramount as clock phase noise can affect a device's performance. A tester with good sources removes the need for dividers or crystals on the DIB. Crystals have good phase noise, but they are not frequency locked to the ATE, so they can cause digital synchronization issues. Thus, you will get better test results if your tester does not require them.

### Test challenges for WiMAX devices

WiMAX devices must undergo a suite of tests to ensure they will operate properly when used in a radio. This range of tests typically includes:

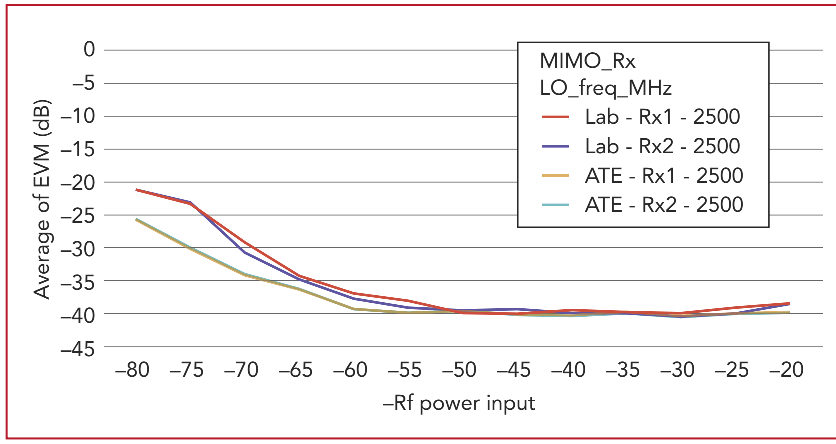
- continuity and leakage tests to ensure correct packaging and electrostatic discharge protection,
- digital pattern tests (including some in scan format),
- traditional INL (integral nonlinearity), DNL (differential nonlinearity), and THD (total harmonic distortion) performance measurements of the converters,
- power-supply consumption measurements for the various operating modes of the DUT, and
- RF receive and transmit operations to test specifications for both sine-wave and modulated signals.

A "loose functional" test may be performed first to determine if the device is alive and if further testing is justified. This step may not be time-efficient, though, depending upon yields and test methodologies.

You may not need to perform the tests in the order shown above, because some testers can perform DSP functions in the background while simultaneously performing other tests, such as ones requiring large digital patterns. Testers that offer such parallel testing can help you optimize the overall test time.

As devices become more complex, it becomes paramount for designers to include design-for-test features in them. For example, a test bus with test modes designed into the DUT assists in the routing of signals to observation points that are not used in normal operation. This visibility assists the test engineer in accurately testing a block or section of the DUT.

## A typical modulation test on the transmission side is EVM.



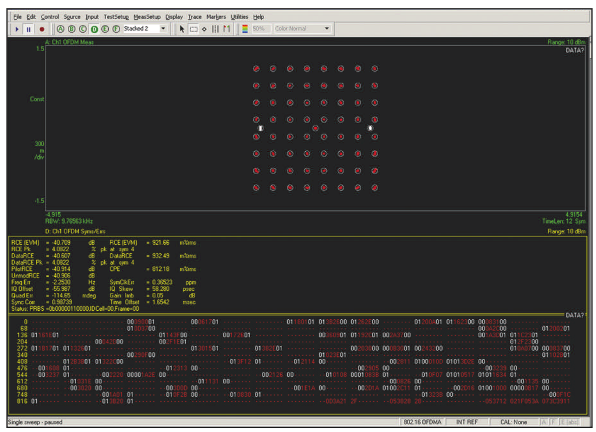



**FIGURE 4.** (top) An Excel spreadsheet provides for easy graphical comparison of ATE and lab EVM data. (bottom) Having common WiMAX EVM constellation display and analysis capabilities in the lab and in production can help lab and production-test engineers work together to deliver samples quickly.

Classical CW (continuous-wave) tests on the transmit RF portion of a WiMAX transceiver include output power, carrier, and sideband suppression measurements. You can also perform a transmit test to measure the LO (local-oscillator) suppression. While this is not a conventional transmit test, you should know how much LO leakage is present at the transmit pin, and is thus being radiated by the antenna. This level is low and the phase noise of the LO cannot be tested using classical CW techniques.

On the receive side, gain, gain linearity, image rejection, and IP3 (third-order intercept) are all key CW tests. RSSI (receive signal strength indicator) is another test you should consider. For RSSI, a device's own indication of the receive level provides a good basic test of receive functionality. The RSSI test usually involves the reading of a register value, a step that can be very handy, especially during wafer probing, when a fully loaded RF tester is often not available and a subset of tests are performed.

### RF modulation testing

Modulated testing looks at the device as it will be used in its final application. This offers the advantage of measuring the performance of the radio as a whole system.

A typical modulation test on the transmit side is EVM (error vector magnitude), also known as RCE (receiver constellation error). EVM measures how far the constellation points are from the ideal; the lower the EVM the better (**Figure 3**).

In a perfect scenario, the constellation points of a modulated signal would be in their ideal locations. But device imperfections resulting from the phase noise of the LO, nonlinearities, image rejection, and other issues cause the constellation points to be in nonideal locations, thus limiting the data rate.

Channel mask testing is another common modulation TX test, where a bandwidth wider than the channel is captured, and the signal level outside the working channel is measured to ensure it is low and inside specification.

For the receive path, tests often measure EVM and BER (bit error rate). The BER is the ratio of the erroneous bits to correct bits—the smaller the better. BER tests measure a modulated RF signal received by the DUT and count the number of the correctly and incorrectly received bits. BER testing has typically been time-consuming because it takes a long time to test very low BER levels.

RF modulation testing can also be used for filter testing. A multitone signal containing a component in the pass band and containing three to six other components in the roll-off and stop bands can be used to quickly determine the 3-dB point and stop-band performance of a device's filters. This multitone signal technique can be used for both RX and TX filters, with a key advantage of only one capture being needed in either the digital or RF domain.

Modulation tests offer useful information about how the DUT will perform in a complete system. DUTs that fail these tests probably won't work satisfactorily. Unfortunately, it is difficult in a production environment to pinpoint which block of the device caused the problem. Both CW testing and modulation testing should be considered necessary to screen out marginal RF performance.

**Bench characterization assistance**

RF devices are characterized on the development bench with lab equipment designed to simulate the operation of the device in final usage and to test the device to the relevant standards. This process is extensive and time consuming and involves a large amount of bench equipment.

Incorporating the same tools in the ATE opens opportunities for the lab and production staffs to work closely together and use the same industry- and RF-standard compliant waveforms and analysis methods. The lab staff will see a reduction in the number of hours they need to spend in the lab, and the production staff will obtain quicker responses to questions on device-setup conditions, register values, and so on.

Today's lab and production staffs can share data more easily than their predecessors, because most newer ATE systems are PC-based and run a Windows operating system. These systems can run tests quickly, over many devices, and can quickly rerun tests with different supply rails if desired, and the test results can be automatically exported to a spreadsheet such as Excel. Engineers can then plot the test results in a graphical form (**Figure 4**), which allows convenient visual analysis and sharing with other team members and management.

Using the same analysis tools in the lab and in production greatly increases the likelihood of correlation between bench and ATE measurements, but skill is still required to deal with factors such as different DUT sockets used in the two locations. In addition, an ATE board will probably be much thicker than a laboratory evaluation board, and supply decoupling locations and RF signal delivery routes will also differ, requiring test engineering skill.

Nevertheless, having a common tool for modulation work can produce an integrated team working less in the lab and more on the tester and delivering engineering samples quicker and in greater volume. Having identical ATE and bench modulation debug displays and setup files is also of great help. The bottom line is the ability to deliver comprehensively tested WiMAX devices in a timely manner that meet customer expectations. T&MW

**Ron Waltman** *is test-development engineering group manager for high-speed signal processing at Analog Devices in Greensboro, NC. He has a BS degree from North Carolina State University.*

**Peter Higgins** *is a staff engineer at Teradyne, where he provides applications support for RF test. He has a BSC degree in electronic engineering from the University of Southampton and a MSc degree in engineering management from the Florida Institute of Technology.*

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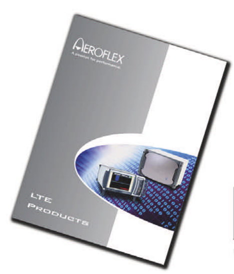


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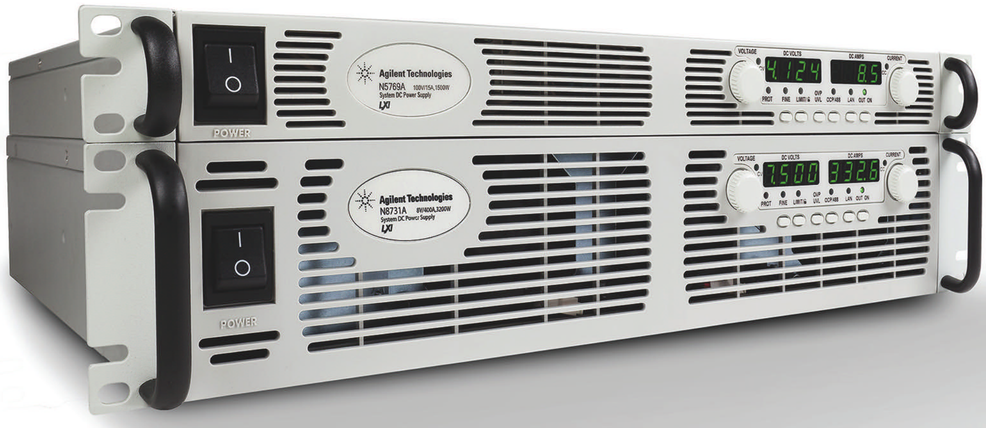


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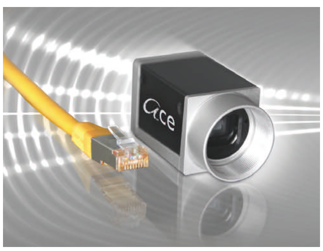
# PRODUCTUPDATE

## Basler debuts low-cost GigE camera

Basler Vision Technologies has introduced the Ace GigE camera, a low-cost, 29x29-mm unit that targets applications now served by analog and FireWire models. The company reports that the Ace camera keeps



costs low, because it requires no frame grabber and can work with low-cost cables and accessories. In addition, the Ace features PoE (Power over Ethernet), allowing one cable to handle data and power, and it also works with Basler's Pylon software, which comes with more than 50 application programming examples to help users start using the camera quickly.

The Ace series will initially consist of four camera models in monochrome and color, with resolutions from VGA to 2 Mpixels and featuring a C-mount adapter. All cameras are equipped with a CCD sensor. The first Ace models will be available in March 2010.

Base price: 299 euros. *Basler Vision Technologies, www.baslerweb.com.*

## JTAG tools support board debug

JTAG Technologies is bringing the look and feel of 20th century debug techniques into the 21st century with a family of products called JTAG Live. The JTAG Live family supports the debugging of boards too crowded for traditional probing and consists of three products:

- Buzz replaces the audible continuity test of traditional DMMs or allows oscilloscope-like probing, checking direct and indirect connections between devices that support boundary scan.
- Clip acts as a logic analyzer, applying vector-based cluster tests.
- Script enables users to employ the Python language to adopt a functional, device-oriented approach to take control of a design through onboard JTAG/boundary-scan-compliant devices.

Instead of addressing the high-volume production-test applications that boundary-scan tools have traditionally served, the three products address debug, small-volume production, and field-service applications, said Peter van den Eijnden, JTAG managing director, who added that the tools don't burden users with netlist requirements. To connect to a board under test, JTAG Live family members are compatible with the JTAG programming cables from Altera and Xilinx as well as with the two-port USB Explorer from JTAG Technologies.

Prices: Buzz—free; Clip—$750; Script—$2250. *JTAG Technologies, www.jtaglive.com.*

## Measure vibration on four channels

The DT8837 sound and vibration instrument from Data Translation lets you measure four accelerometer inputs with 1000-V channel-to-channel isolation. Each channel has a dedicated 24-bit ADC that can sample at 52.734 kHz. The DT8837 is LXI Class C compliant, so it can trigger a measurement based on LAN packets as well as on input levels, software, and an external trigger input.


The instrument has a 24-bit DAC with sample size from 2 ksamples to 128 ksamples. An additional 16-bit feedback ADC lets you monitor the DAC's output. Two 32-bit counters let you measure tachometer, gate, and ADC conversion relationships. The DT8837 also has four digital outputs for driving relays or motors. You can connect up to 16 instruments into a single network to achieve 64 analog inputs.

Price: $3995. *Data Translation, www.datatranslation.com.*

## Monitor 10-Gbps IP networks

As wired and wireless network traffic increases, the need for network monitoring increases along with it. With the introduction of the Iris family of products, Tektronix Communications has enhanced the IP-network-monitoring capabilities of its GeoProbe platform. The new products include the GeoProbe G10, the Iris Analyzer toolset, and IrisView software.

The GeoProbe G10 is a 10-Gbps probe that features a distributed architecture for handling high-bandwidth IP traffic. The Iris Analyzer toolset includes a protocol analyzer, a session analyzer, and a traffic analyzer; it provides layer 2 to layer 7 troubleshooting by characterizing IP traffic by links, applications, and servers. And the configurable IrisView software provides an integrated platform for all applications, including feeds to CEM (customer experience management) systems and third-party applications.

Prices: depend on configuration. *Tektronix Communications, www.tektronixcommunications.com/iris.*

> > > > > > >

## PIM analyzer offers user-selectable Tx frequencies

You can use Boonton's PIM 31 analyzer for testing the PIM (passive intermodulation) of RF components and assemblies. The unit provides two signals up to 20 W each in accordance with the IEC 62037 standard for PIM testing. Carrier power levels are adjustable from +20 dBm to +44 dBm, and transmit frequencies are user-selectable within the analyzer's band.

The PIM 31 analyzer achieves accuracy and sensitivity of –175 dBc at 2x43-dBm carriers, suitable for applications ranging from performance evaluation of RF infrastructure to RF

component testing in the field or on the production floor. Five models are available covering transmit bands ranging from 869 MHz to 2170 MHz and receive bands ranging from 824 MHz to 2060 MHz.

Depending on the application, the PIM 31 can be switched between a functional field-diagnostic mode and a detailed analysis mode. Power and frequency of each transmitted signal can be set individually. You can display up to four intermodulation products—IM3, IM5, IM7, and IM9—and set any up and down sweep frequency range within the unit's bandwidth in 1-MHz increments.

*Boonton, www.boonton.com.*

## Probe card for LCD drivers offers extended life

The GoldTouch from SV Probe is a probe card designed for testing LCD-driver ICs with gold pads. According to SV Probe, the GoldTouch not only improves wafer-level test consistency, but also increases probe-card life, critical for manufacturers of LCD driver devices who are trying to lower test costs. The GoldTouch lowers the cost of probe-card ownership by using a durable probe material to reduce probe-tip wear and damage and thereby extend the life of the probe card.

*SV Probe, www.svprobe.com.*

## PCIe cards provide bus-level timing

Two plug-in cards from Symmetricom offer precise time and frequency functions for computers and servers equipped with the PCI Express bus. The cards can be used for aerospace and defense applications that require microsecond-accurate timing synchronized across multiple computers.

The bc635PCIe and the GPS-synchronized bc637PCIe time and frequency processor cards enable distributed applications to work in

concert and in real time, and they improve the post-processing correlation of collected data. Each card comes with software development kits and drivers for Windows, Linux, and Solaris. The cards also provide extensive time-code generation and translation. Support for IRIG A, B, G, E, IEEE 1344, NASA 36, XR3, and 2137 formats enables the cards to address a variety of timing requirements common to aerospace, defense, and power-utility applications. Applications written for earlier bc635/637PCI cards can be migrated to the new PCI Express cards.

*Symmetricom, www.symmetricom.com.*

## LCR meter has two interfaces

The Z8900 LCR meter from Protek Test and Measurement lets you automate component measurements through its RS-232 and handler interfaces. The 5-digit LCD lets you see C (capacitance), L (inductance), R (resistance), Z (impedance), D (dissipation factor), Q (quality factor), and $\phi$ (phase). The instrument also measures R+Q, L+Q, L+R, C+D, C+R, and Z+$\phi$, and it makes absolute, delta, and delta % measurements. Measurement frequencies are 100 Hz, 120 Hz, 1 kHz, and 100 kHz with basic accuracy of 0.1%. The unit makes 12 measurements/s.

Price: $992. *Protek, www.protek-test.com.*

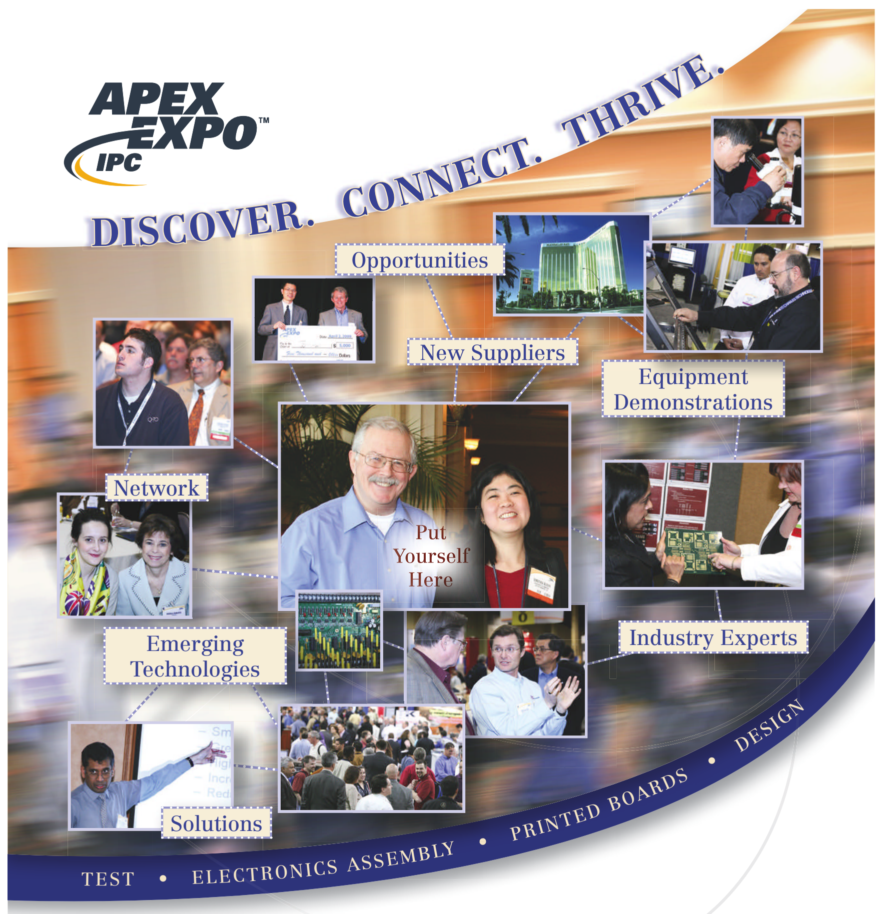
## Switch/measure line gains transient-capture module

Joining VTI Instruments' EX1200 LXI Class A series of configurable switch and measure control subsystems is the EX1200-7416, a transient-capture and time-stamp module with 16 differential channels of analog comparator input. The module supports applications that require level comparison, event detection, and time stamping. What's more, you can configure up to 96 differential channels per full-rack mainframe.

The EX1200-7416 continuously monitors a variety of high-level analog and discrete signals up to 100 V. Each channel employs an 8-bit DAC that can be programmed to set the trip level. Each input signal is also digitally debounced for a programmed time ranging from 1 μs to 500 ms, preventing input signal noise from causing interrupts.

The module records events with IEEE 1588 time codes to provide precise correlation of event and time data. Input channels can be internally routed to an optional DMM to measure the analog level of the signals. The reference DACs can also be routed to the DMM to facilitate self-verification. The EX1200 series can switch up to 576 channels of voltage and temperature in a single rack mainframe.

*VTI Instruments, www.vtiinstruments.com/EX1200.aspx.*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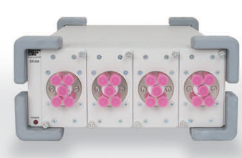

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Test & Measurement World

# MACHINE-VISION&INSPECTION

TEST REPORT

# Multilane AOI speeds PCB inspection

*By Ann R. Thryft, Contributing Technical Editor*

The use of AOI (automated optical inspection) systems with dual-lane configurations is increasing in high-speed PCB (printed-circuit board) assembly, due to the systems' ability to double capacity in the same space without increasing the number of operators. Jean-Yves Gomez, CEO of Vi Technology, commented on how multilane AOI systems are helping to increase yields and speed in PCB inspection, and he explained that such systems are being considered for semiconductor applications as well.

**Q: What does a dual-lane configuration in AOI machines bring to PCB inspection?**

**A:** Today, PCB assembly is massively automated, and productivity is measured by the square meter. Dual-lane configurations have been used in SPI [solder-paste inspection] and pick-and-place inspection for a couple of years, although they are not yet widespread in PCB inspection.

Adding more lines to increase capacity would normally require more operators and more floor space. A dual-lane AOI configuration consists of two side-by-side, width-adjustable conveyors that can inspect PCB assemblies in each of the lanes. Aside from the extra lane, you may also add another camera. So, it requires the same floor space and the same number of operators as a single-lane AOI machine but doubles capacity. The other immediate benefit is an increase in speed of roughly 30%.

Dual-lane inspection also gives flexibility. Operators can work in parallel with two different products, each with a different set of inspection criteria. A large manufacturer could use both lanes to increase inspection volume for one product, while a small manufacturer could maximize space by using each lane for a different product.

## INSIDE THIS REPORT



**Q: Is this technology also applicable to semiconductor inspection?**

**A:** We're getting requests from semiconductor companies for more complex inspection solutions. They are facing severe constraints in back-end inspection as IC package complexity rises. For example, the wire bonding in all of the multiple, stacked die in a cellphone baseband module must be verified. In some cellphone camera modules, the die contains actuators and lenses, so die cost can represent half of the module cost. It's important to get 99% yield in the back end, so most of the time semiconductor companies use visual inspection. As many as 200 operators per shift may look at the die before it is packaged.

Jean-Yves Gomez
CEO
Vi Technology

But defects are getting too small for the human eye to see accurately and quickly, even using microscopes. One semiconductor manufacturer has approached us about using a dual-lane configuration for inspecting two different camera modules, a 3-Mpixel module on one lane and a 5-Mpixel module on the other.

**Q: What kinds of floor space constraints are manufacturers facing?**

**A:** Especially in China, the cost of floor space is rising. All of those plants are clean rooms, and the cost per square meter is very high. One dual-lane AOI machine in 1 $m^2$ could replace 40 to 50 manual operators in 100 $m^2$ of a clean room.

**Q: What other trends are affecting AOI throughput?**

**A:** Multisegment conveyors can optimize dual-lane loading. For example, with very small boards, you can use them to pre-load a panel to save time. For very high-volume environments, we are investigating some quad-lane configurations created by placing dual-lane machines back to back. □

EDITOR'S NOTE

## The need for speed

*By Ann R. Thryft,*
*Contributing Technical Editor*

In both good and bad economic times, OEMs need to increase productivity by boosting efficiency, cost-effectiveness, and sometimes just plain volumes. Makers of machine-vision systems and components are working to continuously improve their products and technologies so they help enable these goals. One thing they all have in common is the push to increase throughput, whether that's measured in how many PCB (printed-circuit board) assemblies an AOI (automated optical inspection) machine can inspect per minute or in the number of hours it takes to produce a 6-in. photovoltaic solar wafer.

But meeting the need for speed isn't enough. New or improved technologies not only have to be better; they must also be tailored so they can be easily integrated with what's already on the factory floor.

For example, although dual-lane configurations are a relatively new thing in PCB assembly inspection with AOI systems, these configurations have already been doubling productivity rates in SPI (solder-paste inspection) and pick-and-place machines (p. 61). And as defects continue to shrink in size, the technology may be coming soon to semiconductor inspection, too. In solar-cell inspection, SEM (scanning-electron microscope) and FIB (focused ion beam) technologies can be applied to submicron solar characterization (p. 68), but until their throughput improves, dual-beam systems are limited to offline sampling use in solar. □

*Contact Ann R. Thryft at ann@tmworld.com.*

HIGHLIGHTS

## Qioptiq unveils vision metrology system

Able to zoom across its 12.5:1 magnification range in less than 1 s, the Fetura noncontact vision metrology system from Qioptiq approaches the speed of digital zoom lenses without the loss of resolution inherent in digital zooms, according to the manufacturer. Fetura's PowerMetrix software provides color edge detection and includes tools for image processing, coordinate data acquisition, and geometric calculation. The all-LED illumination is programmable for intensity, direction, and angle of incidence. The Fetura system comes in four models, with stage travel ranging from 200x200x200 mm to 800x800x250 mm. www.qioptiqlinos.com.

## Cameras offer fast frame rates

Outfitted with Kodak's progressive-scan interline CCD image sensors with Quad-Tap technology, the SX series of cameras from Baumer targets industrial applications requiring resolutions of 1, 2, or 8 Mpixels at rates of up to 120 fps. All SX cameras have a base Camera Link interface and are available in both monochrome and color versions. To simplify the integration of these cameras into existing operating software, Baumer offers a software development kit containing a generic application programming interface, code examples, and programming documentation. www.baumer.com.

## Cognex expands vision software

Release 6.0 of VisionPro hardware-independent software from Cognex adds support for very large camera images and nonconventional sources. In addition, VisionPro 6.0 offers calibration and image correction for line-scan cameras and expanded ID reading capability for 2-D codes.

The software can now acquire images up to 16 bits in depth, which enables the use of sources such as 3-D profilers, thermal cameras, and x-ray imagers. Release 6.0 also works with Microsoft 64-bit operating systems, which allows it to accommodate larger cameras and greater pixel depth.

Also new is a high-accuracy calibration tool for use with line-scan cameras. A single calibration-board image is sufficient for correcting camera distortion and camera displacements, such as rotation and tilt. Finally, VisionPro's ID symbol reader now reads 2-D codes up to 144x144. www.cognex.com.

## Frame grabber fits ExpressCard slot

The PIXCI ECB1-34 from EPIX is a base Camera Link frame grabber that plugs into an ExpressCard/34 or ExpressCard/54 slot in a notebook computer and boasts sustained transfer rates of 200 Mbytes/s and burst transfer rates of up to 250 Mbytes/s. You can use the frame grabber with line-scan or area-scan cameras operating in either free-run (continuous) or controlled (triggered) mode. The PIXCI ECB1-34 offers software-selectable bit packing to decrease the data rate to the ExpressCard bus and to conserve storage space when capturing 10-bit or 12-bit pixels.

The companion XCAP software comes in three versions: Lite, LTD, and STD. XCAP-Lite provides camera control and image capture with no software development. It is limited to a 64-Mbyte frame buffer. XCAP-LTD supports up to a 4-Gbyte frame buffer on 32-bit operating systems or an 8-Gbyte frame buffer on 64-bit operating systems. XCAP-STD adds video-to-disk capture limited only to the size and speed of the hard-drive system and can capture to the limit of the available notebook memory. www.epix.com.

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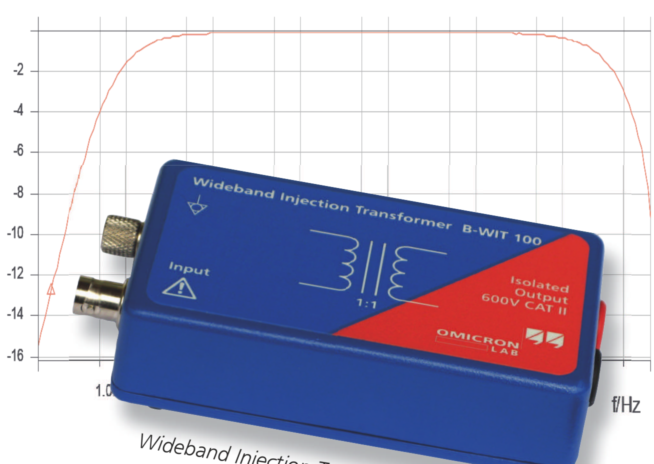


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# CCD and CMOS sensors become more finely tuned

*By Ann R. Thryft, Contributing Technical Editor*

Many of the characteristics that engineers look for in machine-vision cameras are determined by the image sensor at the heart of that camera. High-quality images, high resolution, high frame rates, greater sensitivity to light, and the ability to capture moving images without distortion are all dependent on CCD or CMOS sensor chips.

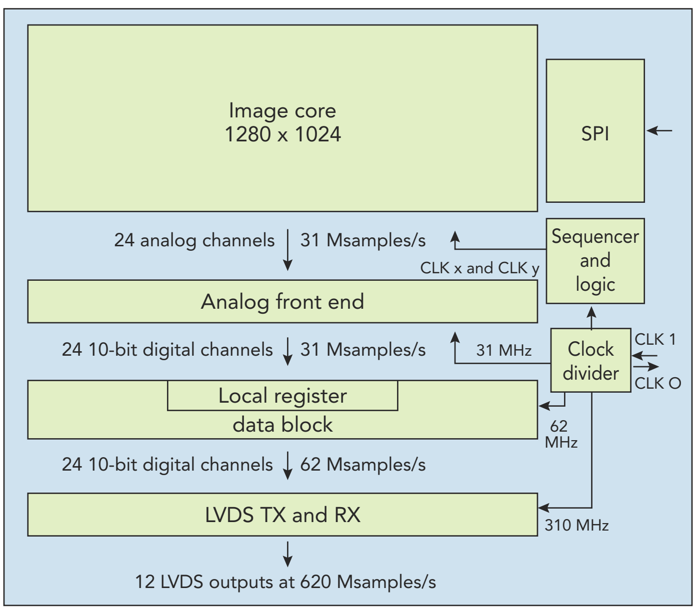
Typically, the main goal in machine vision is not to acquire the perfect picture but to extract the right information for the application in which the imaging system is used, said Danny Scheffer, director of business development for custom imaging sensor products for Cypress Semiconductor, a maker of CMOS sensors. Examples of that information are the presence or absence of components on a board, the location and orientation of a component in an assembly, the type of component, and the information stored in labels. "The application sets the characteristics of the sensor to be used, including variables such as speed requirement, device size, light source, and whether the light environment is controlled," he said. "All of these in combination determine [what you need to look for in] pixel size, resolution, frame rate, and shutter type."

A quick comparison of CCD and CMOS sensors would find that CCD sensors, which can offer resolutions as high as 22 Mpixels, provide higher image quality at a correspondingly higher price. In contrast, the lower-cost CMOS sensors, with their much smaller 1-Mpixel to 4-Mpixel resolutions, capture images more quickly, which is desirable in a high-speed production line.

In applications where the highest image quality is needed, such as wafer and mask inspection, customers are willing to pay the higher price of CCD sensors. CCD technology produces higher-quality images because it was developed specifically for imaging, said Michael DeLuca, marketing manager for Eastman Kodak's Image Sensor Solutions group, a maker of CCD sensors. "In order to make CMOS capable of imaging, it had to be adapted to make it sensitive to light," he said.

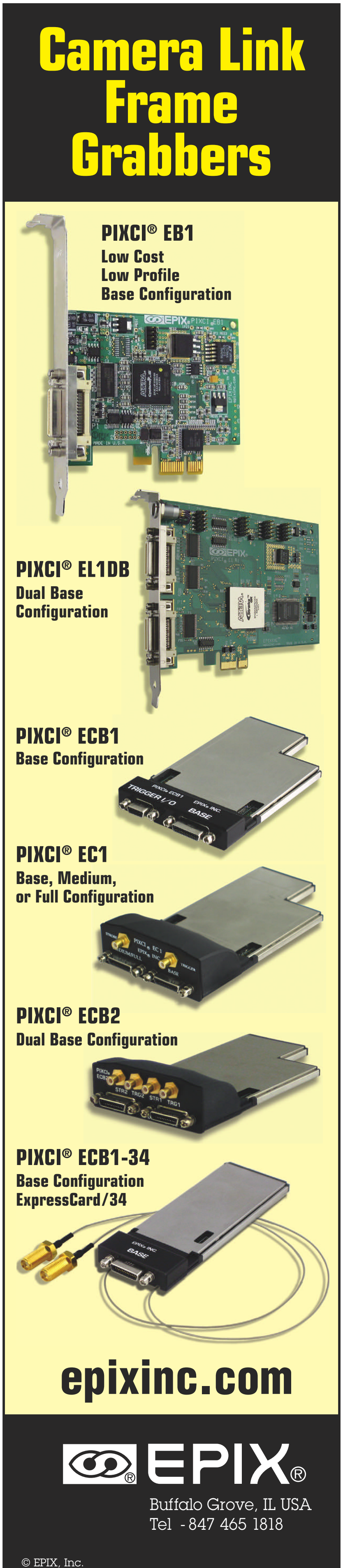
While the camera's frame rate is important in maintaining productivity as objects move down an assembly line, so is the time it takes to process an image. "Cameras used in these applications tend to include only limited post-processing circuitry, since you want to analyze the image as quickly as possible, rather than spend time to fix the image first," DeLuca said. "As a result, the CCD sensors we sell to this market tend to be of very high quality. This is one reason that CCD technology continues to have a good presence in these markets: It can provide very high-quality images directly from the sensor."

The electronic shutter that is inherent in progressive-scan, interline-transfer CCDs is also important in inspection applications because it eliminates the need for a moving part—a mechanical shutter—by providing clean image capture of moving objects, said DeLuca. "This is a real advantage of CCD image sensors, as CMOS devices are susceptible to artifacts such as image skew when using a rolling shutter."




**The 1.3-Mpixel LUPA 1300 CMOS sensor has 12 high-speed outputs, windowing capability, and a fully synchronous snapshot shutter that makes it possible to capture images of moving objects without distortion and to read one image while the next one is being acquired.** Courtesy of Cypress Semiconductor.

Nevertheless, CMOS chips have made great strides in electronics and semiconductor inspection because they can deliver higher imaging speeds at a lower cost in applications such as laser profiling on flip-chip and BGA (ball-grid array) packages, said David Cochrane, director of product management and marketing for Dalsa, which makes both types of sensors. Cochrane pointed out, though, that although CMOS delivers a lower cost of implementation than



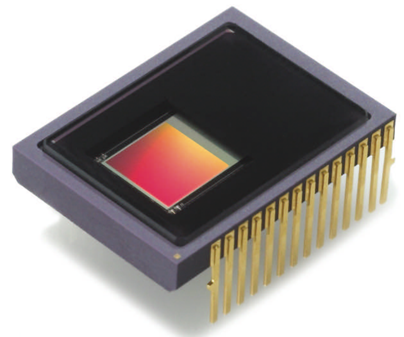

CCD, there are fewer CMOS models to choose from because they are newer in the industry.

Joost Seijnaeve, Cypress Semiconductor's marketing director for standard imaging products, concurred with Cochrane's assessment of the market. "The data quality of CMOS has improved," he said, "and combined with its integration ability, CMOS sensor technology is taking market share away from CCD technology." Seijnaeve explained that because CCD sensors can't remove the charge as fast as is needed in high-speed imaging, phenomena like ghosting can occur. In addition, CCD sensors also have much higher power-dissipation levels than CMOS devices.

Cliff Drowley, VP of Cypress Semiconductor's imaging business unit, explained that the historical advantage of CMOS has been the fact that all of the timing and analog signal chain circuitry can be integrated onto the same chip as the sensor array, simplifying the bill of materials and minimizing camera size. "CMOS frame rates are also faster, since you can do pipelined shutter schemes," he said. Because of the nature of clocking in CCDs, it's extremely difficult to use them for implementing high-speed cameras. CCDs are not as good as CMOS sensors at performing high-speed capture or high-speed data transfer off of the device.

In order to get high frame rates in CMOS sensors, many parallel outputs are required, from 64 to 128 or more, just to get the data off-chip. "The pixel types for high-speed global, or snapshot, shutters are very specialized," he said. For very high-speed applications of several thousand frames per second, sensors also incorporate a pipelined global shutter. This consists of on-pixel storage circuitry, so that one frame can be captured while the previous frame is read out.

"We also aim at optimizing the sensor's modulation transfer function, which is a measure of the sharpness of the image detected on the sensor, for machine vision and particularly



**Dalsa's 1-Mpixel, FT50M progressive-scan CCD sensor can read out 1k x 1k pixels at 50 fps, has a high linear dynamic range of 67 dB at 40 MHz, and has a second output for mirrored or split readout.** Courtesy of Dalsa.

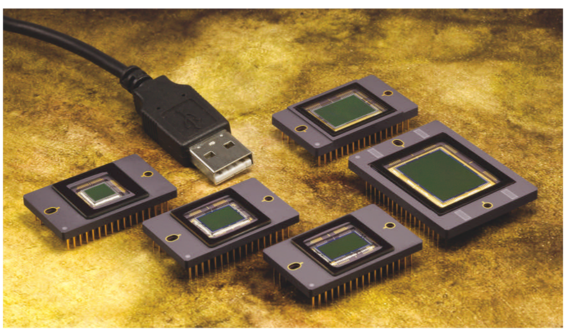
for high-speed designs," said Drowley. "To expand the dynamic range of CMOS sensors so they can adapt to different light levels, we can program a nonlinear response curve on the sensor."

Drowley said that CMOS is also closing the gap in another area where CCD sensors have had a major advantage: noise level. Until the late 1990s, CCD had the advantage over CMOS in the way the charge was read out. CCD sensors could eliminate a lot of temporal noise by using correlated double sampling, he said. "In 1998, the first commercial CMOS imagers with true correlated double sampling for noise appeared. In many applications today, noise performance is equivalent in CMOS and CCD technology."

## Trends in image sensors

Customers want electronic shutters and the speed of CMOS, but they also want high image quality, lower read noise, and higher sensitivity for the more demanding applications, said Dalsa's Cochrane. Some customers are demanding larger-sized pixels to increase a sensor's sensitivity, because as inspection speed increases, light, and therefore the signal, becomes more difficult to capture, he said. "The recent trend to smaller pixel sizes in consumer imaging does not fit well in the industrial segment, since many of these devices have higher pixel defect rates and are only suited to the more basic inspection tasks. Electronics and semiconductor inspection demands the highest image quality, and some applications require perfect imagers.”

Although big pixels can store more charge, increase the dynamic range, and lower the noise floor, small pixels may be needed to get enough of them in a particular optical format, said DeLuca. “Many of the qualities needed in an image sensor can’t be optimized in the same directions,” he said. “For example, high resolution requires high pixel counts, but it then takes additional time to read out those extra pixels, lowering frame rate.” DeLuca said that in Kodak’s newest family of interline CCD image sensors, pixel area size has been reduced by about 50% from the previous generation, while performance has been maintained and even improved in some areas, such as frame rate and image smear.



**In Kodak’s newest family of interline CCD sensors, the 4-Mpixel and 8-Mpixel devices support a region of interest mode that allows the center portion of the sensor to be read out at higher frame rates.**

Courtesy of Eastman Kodak.

Today, the demand is for machine-vision sensors with 90 to 100 fps at about 1.3 Mpixels, and in the near future, demand will be for 100 to 200 fps and 2 Mpixels, said Seijnaeve of Cypress. “The next generation of machine-vision sensors will require frame rates above 100 fps, resolutions of 3 Mpixels or higher, standard optical formats of 1/2 in. to 2/3 in., low-light sensitivity, high dynamic range, global shutters, and windowing.”

Sensor improvements that Cypress is working on now include enhancing image quality, increasing optical dynamic range, and increasing functionality and flexibility, Scheffer said. The company is also integrating post-processing functions, such as ADCs and gain amplifiers, timing generators, and everything else that’s needed for easy integration of the sensor into the end system.

“The next step will be more configurability, or programming, on the sensor,” said Scheffer. “In the future, we expect to integrate color construction and pixel-correction algorithms. CMOS image sensor features are moving from image improvement toward the integration of more image-processing and post-processing features.”

Resolutions greater than 10 Mpixels are the latest trend in CCD and CMOS area devices, said Cochrane. “Linescan CCDs still rule and have reached 12k and even 16k pixels in custom models,” he said. But in the near future, standard image capture technology will exceed 1 Gpixel/s, which is faster than the data transfer rates of current frame grabbers and PC interfaces. “As sensors become this fast, you won’t be able to send data to the PC at the rate it’s being acquired,” Cochrane explained.

Because in machine vision there’s usually a region of interest and certain specific information users need to get from the image, Cypress sees a trend toward sensors that incorporate image-processing algorithms that let you extract only the data you want, said Drowley. “This processing capability entails integrating a lot more digital circuitry on the sensor itself, which CCD sensors can’t do, but which CMOS technology does well. Right now, this is a relatively small piece of the machine-vision space, but it looks like something that will grow.” □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# Subsurface solar-cell characterization

*By Ann R. Thryft, Contributing Technical Editor*

Inspection methods such as x-ray, laser, and photoluminescence can scan photovoltaic solar cells and wafers for surface defects. But engineers at firms that manufacture solar cells also must detect and localize subsurface defects such as microcracks in substrates, crystalline dislocations, and micro-shunts, said Vinh Van Ngo, MEMS/Solar/LED business development manager for FEI. In addition, the engineers need to simultaneously locate and measure submicron features for detailed structural and process analyses. Because dual-beam systems—a SEM (scanning-electron microscope) combined with a FIB (focused ion beam)—can find subsurface and submicron defects, equipment makers such as FEI are applying them to the material characterization and inspection needs of PV (photovoltaic) solar cells, said Ngo.

"Regular, unenhanced optical imaging doesn't penetrate through the substrate, while x-ray imaging techniques are limited in the amount of contrast and resolution they provide and thus in the amount of information you can get about subsurface defects," said Ngo. Optical techniques, including laser and photoluminescence, are primarily surface inspection techniques with limited resolution, and therefore cannot see critical thin-film or crystalline structures at dimensions below 1 micron.

SEMs, however, are well known in both R&D labs and production facilities for their nanometer-level imaging ability, as well as for their wide imaging range and material analytical capabilities. FIB technology is a long-established technique for milling, shaping, and modifying to reveal subsurface detail or to construct material structures at the micron and nanometer scales.

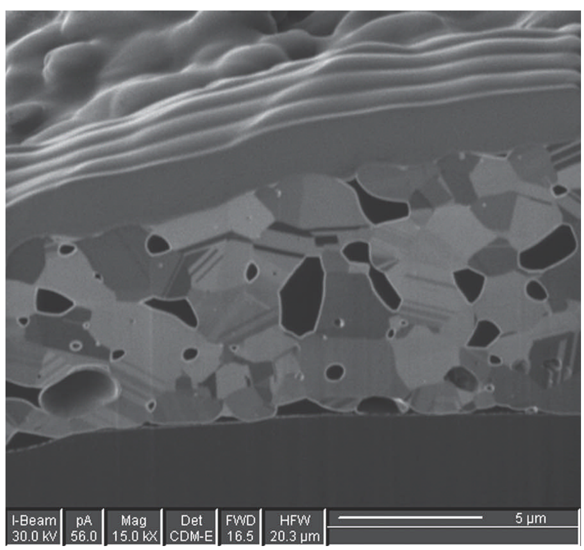


**Fig. 1** **This cross-section image shows grain boundaries and voids on a silicon photovoltaic cell contact, with contrast enhanced by the ion-channeling effect of focused ion beam imaging.**
Courtesy of FEI.

Ngo said that FEI is combining SEM and FIB technologies to address both thin-film and crystalline silicon PV solar cells on the manufacturing floor. The bulk of PV solar-cell manufacturing capacity is crystalline silicon-based, in either polycrystalline or monocrystalline forms.

Subsurface, submicron defects in crystalline PV solar cells include voids at contacts (**Fig. 1**), micro-shunts, cracks, and dislocations (crystalline wafer imperfections). Thin-film defects include voids at contacts, as well as delamination, micro-shunts, and dislocations (primarily lattice mismatches).

In R&D, SEMs have traditionally been used for imaging and metrology of surface features as small as 10 nm, and, in conjunction with FIBs, of subsurface features. FIBs have also proven useful for sample preparation for higher-resolution analysis using STEM (scanning-transmission-electron microscope) technology and for material composition analysis using energy-dispersive x-ray spectroscopy, according to Ngo. "Tool sets that address PV-specific challenges can be adapted from the ones commonly used for nanotechnology and semiconductors," he said. The ability to methodically and accurately locate defects that impact performance efficiencies, and therefore the cost per watt, of PV cells has previously been available only in a laboratory setting.

Scientists and engineers at R&D centers and service labs are already using the dual-beam SEM/FIB combination for solar-cell inspection, characterization, or metrology. "The challenge is to demonstrate the technologies' scalability, familiarize people with [the technologies], and make them easier to use," said Ngo. "Traditionally, the tools used by R&D staff require a highly trained operator. That's OK in a laboratory, but a production-support environment requires instruments that are faster and easier to use. We need to create automated tools that simplify and streamline applications for PV production support engineers, scientists, and developers who are not already familiar with SEMs and FIBs."

These users need a semiautomated PV tool that uses a SEM column to scan PV samples or wafers sampled from the production line (**Fig. 2**) and generate charge carriers within them to detect defects, said Ngo. The corresponding scan profile of measurements of EBIC (electron-beam-induced current) provides target site locations for detailed examination or further micro-analysis using a FIB on the same system. This technique pro-


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vides the subsurface data needed to evaluate or verify the PV production process's quality and parameters, said Ngo.

In PV, this type of dedicated dual-beam is still limited by throughput, approximately 3 to 5 hr per 6-in. wafer, so it is not practical as an in-line technique. Instead, it must operate in parallel with the production process to provide near-production sampling, said Ngo.

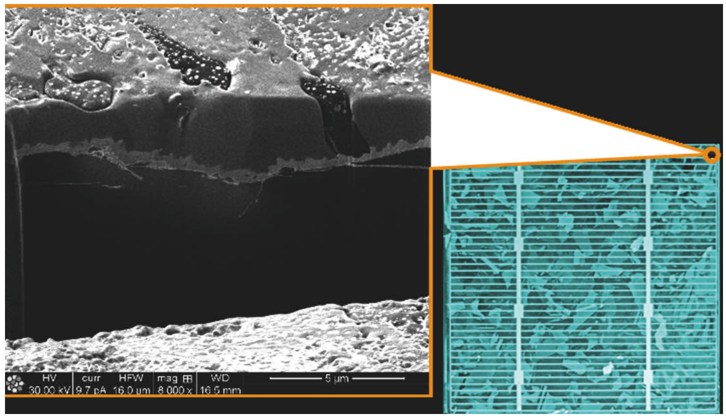
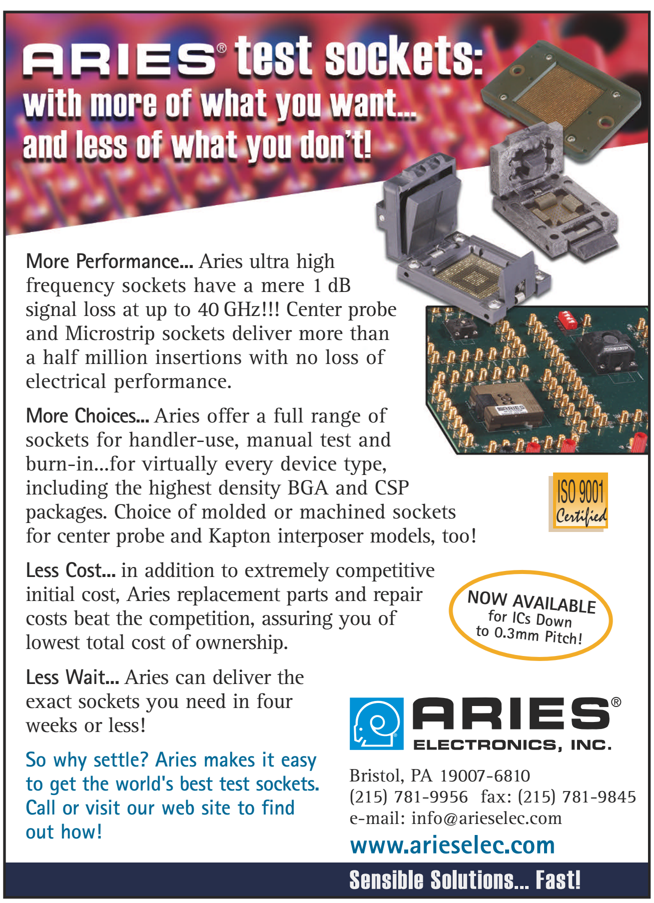


**Fig. 2** This focused ion beam cross-section of a PV solar cell depicts the nano-level details of macro-level defects detectable by a semi-automated electron-beam-induced-current system.
Courtesy of FEI.

"We are confident that these technologies can ultimately provide the speed and depth of data needed for near-line production support. These capabilities will play a critical role in silicon-based and thin-film-based PV manufacturers' efforts to achieve cost parity with other energy sources," he said.

Changes are also coming in solar-cell technology, such as new substrate and thin-film materials for higher device efficiency. These will necessitate better definition of defects and features of interest, as well as better sampling requirements for production and R&D, and new metrics, according to Ngo. He added, "These are all part of a new global PV standards roadmap effort by the Department of Energy and SEMI's newly founded PV Group initiative." □

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## BUSINESS STAFF

**Publisher:** Russell E. Pratt, rpratt@reedbusiness.com

**Associate Publisher:** Judy Hayes, judy.hayes@reedbusiness.com

**Director, Custom Programs and Solutions:** Karen Norris-Roberts, knorris@reedbusiness.com

**Online Account and Marketing Manager:** Melanie Turpin, melanie.turpin@reedbusiness.com

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# VIEWPOINT

[An exclusive interview with a technical leader]

**HIROMICHI TODA**
President
Anritsu
Atsugi, Japan

Hiromichi Toda joined Anritsu in 1971 after graduating from the Waseda University Department of Science and Engineering. He has held engineering and general business management positions in Anritsu's Kanagawa, Japan, headquarters, as well as at the US subsidiary in Morgan Hill, CA. He was appointed senior VP and GM of Anritsu's measurement business group in June 2004 and assumed the role of president in June 2005.

Contributing editor Larry Maloney conducted an e-mail interview with Hiromichi Toda on instrumentation for the communications market and other specialized applications.

## Wireless: prime engine for communications test

**Q: How do you assess the recovery in the global communications test market?**

**A:** Demand for measuring instruments for installation and maintenance of 3G wireless infrastructure is robust, especially in the US and Asia. We also see growing demand for measuring instruments used in LTE development, particularly in Europe, the US, Korea, and Japan. However, the market for measuring instruments for telecommunications has not yet recovered. Global production of mobile phones, for instance, remains below the 2008 level, and test equipment investment is weak in that area as a result. On the other hand, telecommunications for public safety and homeland security in the US is increasing. China, Latin America, and Africa also promise healthy growth for Anritsu as they build out their networks.

**Q: What's the status of next-generation wireless systems?**

**A:** There is potential demand for HSPA+ (evolved high-speed packet access) from manufacturers in Europe and the US. For WiMAX, we see rising demand for measuring instruments used in development and manufacture of RF components. LTE is scheduled to be commercialized in several regions in 2010. For that market, we introduced our MD8430A signaling tester a year ago, and it has been well received by chipset and terminal vendors. Anritsu was involved very early in development of LTE, and we now have a complete portfolio of test instruments used in the design and manufacture of LTE devices, handsets, and systems. For example, we introduced the first LTE handheld test solution, the BTS Master, now being used for early testing and deployment of LTE networks.

**Q: What is distinctive about Anritsu's communications test technology?**

**A:** Our customer base consists of major telecommunications carriers and telecommunication equipment manufacturers, and we've introduced industry leading products by answering their needs. For example, we commercialized the world's first OTDR (optical time-domain reflectometer) for fiber-optic applications, and we led the way with the introduction of a handheld OTDR for onsite use. Other innovations have included: an all-in-one SONET/SDH tester, a 3G signaling tester, and a handheld analyzer for wireless infrastructure. Anritsu's strength lies in its accumulated technology covering both wire and wireless telecommunications. We've developed instruments for cutting-edge development and maintenance applications, as well as protocol analysis technology that locates and identifies problems in increasingly sophisticated networks.

**Q: How much focus does Anritsu place on developing specialized instruments?**

**A:** Anritsu's philosophy is to offer first-to-market product innovations and services. The MW90010A Coherent OTDR, which detects faults in submarine optical cables, is a prime example of an innovative product that responds to the needs of the market. Another example is in the LTE area, where our new MF6900A simulates fading by delaying and reflecting radio waves. By connecting it to an MD8430A signaling tester that simulates a 3GPP (3rd Generation Partnership Project) LTE base station, you can test fading in a 2x2 MIMO (multiple input, multiple output) environment. This is essential for developing and validating 3GPP LTE terminals and chipsets. We'll continue to use our expertise for development of such niche products, as well as to contribute on a global basis to expanding communications technology. T&MW

Hiromichi Toda answers more questions on communications test and innovation at Anritsu in the online version of this interview: www.tmworld.com/2009_12.

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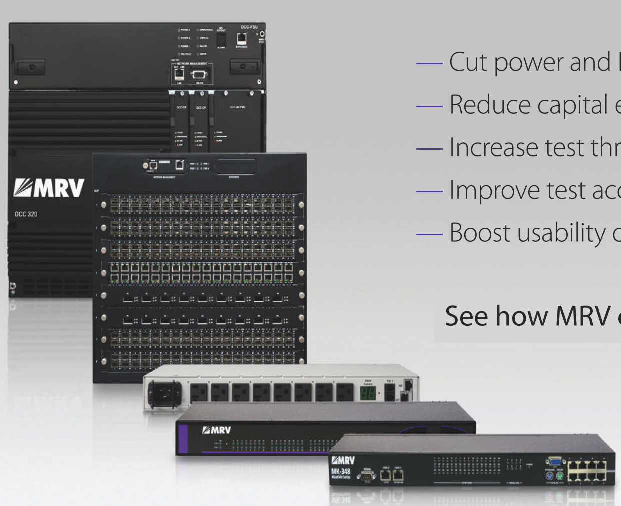


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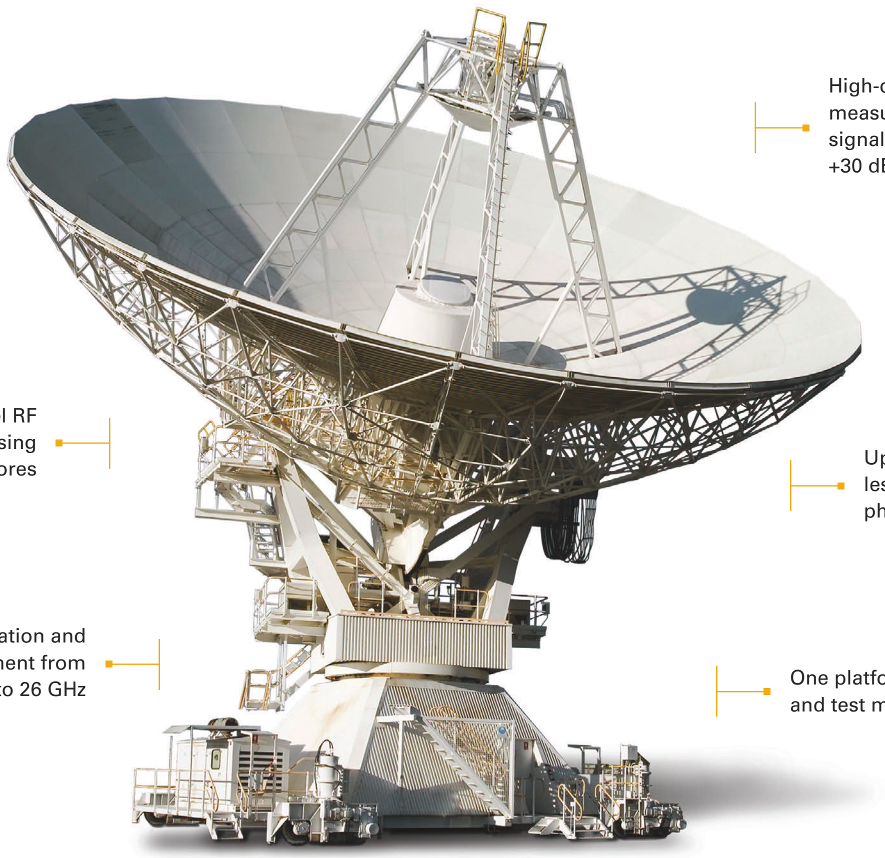


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